

TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

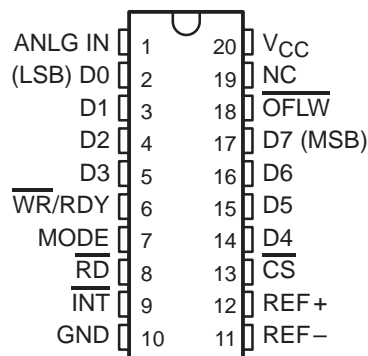
SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
Read Mode . . . 2.5 μ s Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track and Hold**
- **Single 5-V Supply**
- **TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

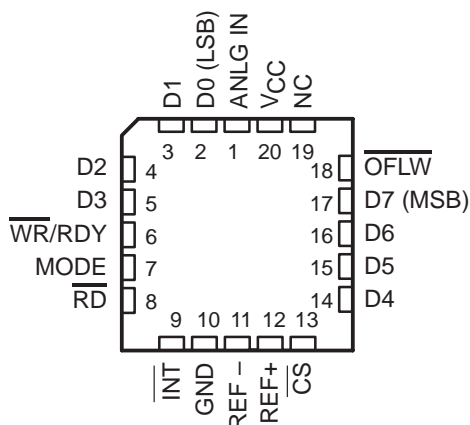
description

The TLC0820AC and the TLC0820AI are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified flash technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μ s over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/ μ s without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

**DB, DW, OR N PACKAGE
(TOP VIEW)**



**FN PACKAGE
(TOP VIEW)**



NC—No internal connection

AVAILABLE OPTIONS

T _A	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
–40°C to 85°C	±1 LSB	—	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

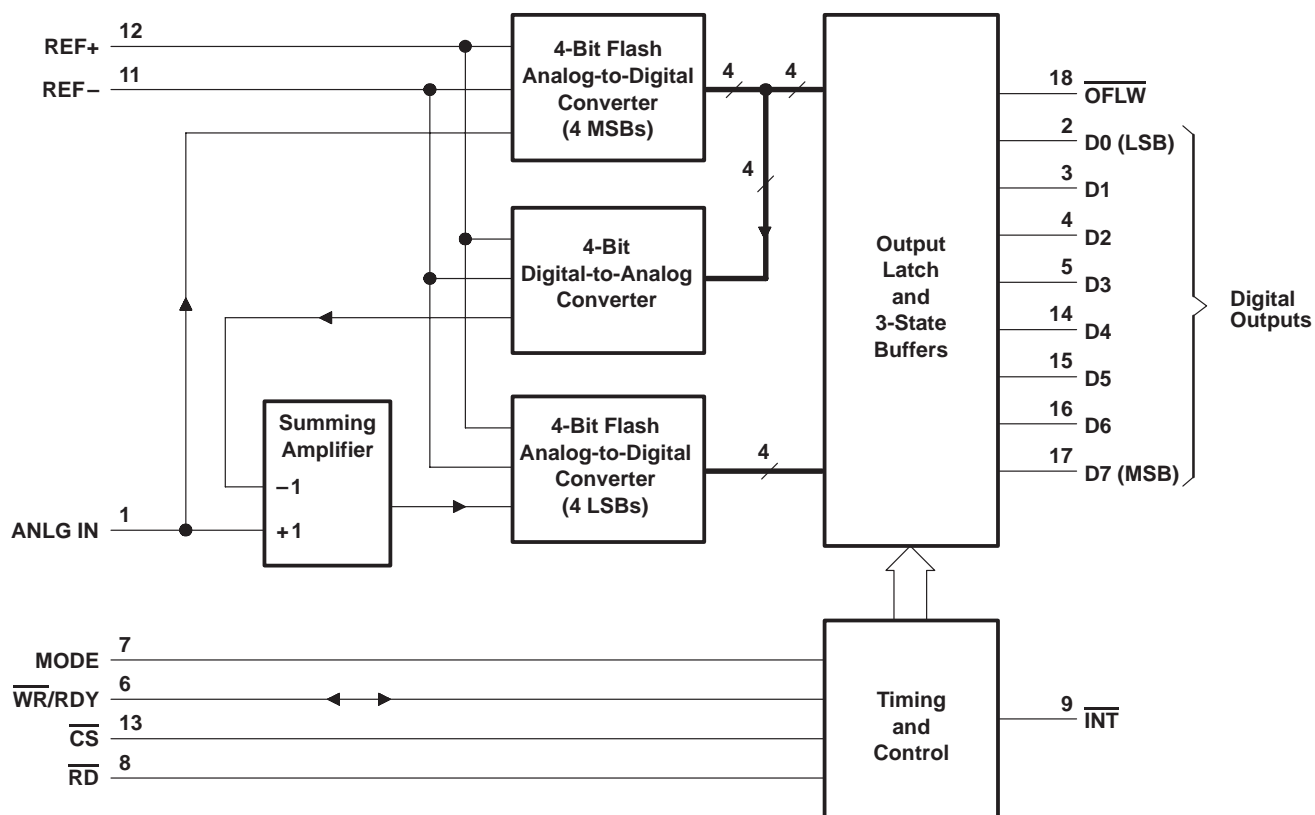
Copyright © 1994, Texas Instruments Incorporated

TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

functional block diagram



TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG IN	1	I	Analog input
$\overline{\text{CS}}$	13	I	Chip select. $\overline{\text{CS}}$ must be low in order for $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
$\overline{\text{INT}}$	9	O	Interrupt. In the write-read mode, the interrupt output ($\overline{\text{INT}}$) going low indicates that the internal count-down delay time, $t_{d(\text{int})}$, is complete and the data result is in the output latch. The delay time $t_{d(\text{int})}$ is typically 800 ns starting after the rising edge of $\overline{\text{WR}}$ (see operating characteristics and Figure 3). If $\overline{\text{RD}}$ goes low prior to the end of $t_{d(\text{int})}$, $\overline{\text{INT}}$ goes low at the end of $t_{d(\text{RIL})}$ and the conversion results are available sooner (see Figure 2). $\overline{\text{INT}}$ is reset by the rising edge of either $\overline{\text{RD}}$ or $\overline{\text{CS}}$.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50- μA current source, which acts like a pulldown resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
$\overline{\text{OFLW}}$	18	O	Overflow. Normally $\overline{\text{OFLW}}$ is a logical high. However, if the analog input is higher than $V_{\text{ref+}}$, $\overline{\text{OFLW}}$ will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
$\overline{\text{RD}}$	8	I	Read. In the write-read mode with $\overline{\text{CS}}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{\text{RD}}$ goes low. $\overline{\text{RD}}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{\text{RD}}$. In the read mode with $\overline{\text{CS}}$ low, the conversion starts with $\overline{\text{RD}}$ going low. $\overline{\text{RD}}$ also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and $\overline{\text{INT}}$ going low indicate completion of the conversion.
REF–	11	I	Reference voltage. REF– is placed on the bottom of the resistor ladder.
REF+	12	I	Reference voltage. REF+ is placed on the top of the resistor ladder.
VCC	20		Power supply voltage
$\overline{\text{WR}}$ /RDY	6	I/O	Write ready. In the write-read mode with $\overline{\text{CS}}$ low, the conversion is started on the falling edge of the $\overline{\text{WR}}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(\text{int})}$, provided that the $\overline{\text{RD}}$ input does not go low prior to this time. The delay time $t_{d(\text{int})}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of $\overline{\text{CS}}$ and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL

CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage range, all inputs (see Note 1)	–0.2 V to $V_{CC}+0.2$ V
Output voltage range, all outputs (see Note 1)	–0.2 V to $V_{CC}+0.2$ V
Operating free-air temperature range: TLC0820AC	0°C to 70°C
TLC0820AI	–40°C to 85°C
Storage temperature range	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DB, DW or N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}			4.5	5	8	V
Analog input voltage			−0.1		V _{CC} +0.1	V
Positive reference voltage, V _{ref+}			V _{ref−}		V _{CC}	V
Negative reference voltage, V _{ref−}			GND		V _{ref+}	V
High-level input voltage, V _{IH}	V _{CC} = 4.75 V to 5.25 V	$\overline{CS}, \overline{WR/RDY}, \overline{RD}$	2			V
		MODE	3.5			
Low-level input voltage, V _{IL}	V _{CC} = 4.75 V to 5.25 V	$\overline{CS}, \overline{WR/RDY}, \overline{RD}$	0.8			V
		MODE	1.5			
Pulse duration, write in write-read mode, t _{w(W)} (see Figures 2, 3, and 4)			0.5		50	μs
Operating free-air temperature, T _A	TLC0820AC		0		70	°C
	TLC0820AI		−40		85	



TLC0820AC, TLC0820AI

**Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES**

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

electrical characteristics at specified operating free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T _A [†]	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	D0–D7, $\overline{\text{INT}}$, or $\overline{\text{OFLW}}$	V _{CC} = 4.75 V, I _{OH} = −360 μA	Full range	2.4			V
			V _{CC} = 4.75 V, I _{OH} = −10 μA	Full range	4.5			
				25°C	4.6			
V _{OL}	Low-level output voltage	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR/RDY}}$	V _{CC} = 5.25 V, I _{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I _{IH}	High-level input current	$\overline{\text{CS}}$ or $\overline{\text{RD}}$	V _{IH} = 5 V	Full range		0.005	1	μA
		$\overline{\text{WR/RDY}}$		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range		200		
25°C		50	170					
I _{IL}	Low-level input current	$\overline{\text{CS}}$, $\overline{\text{WR/RDY}}$, $\overline{\text{RD}}$, or MODE	V _{IL} = 0	Full range		−0.005	−1	μA
I _{OZ}	Off-state (high-impedance-state) output current	D0–D7 or $\overline{\text{WR/RDY}}$	V _O = 5 V	Full range			3	μA
			25°C		0.1	0.3		
			V _O = 0	Full range		−3		
25°C		−0.1	−0.3					
I _I	Analog input current		CS at 5 V, V _I = 5 V	Full range			3	μA
				25°C			0.3	
			CS at 5 V, V _I = 0	Full range			−3	
				25°C			−0.3	
I _{OS}	Short-circuit output current	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR/RDY}}$	V _O = 5 V	Full range		7		mA
				25°C		8.4	14	
		D0–D7 or $\overline{\text{OFLW}}$	V _O = 0	Full range		−6		
				25°C		−7.2	−12	
		INT		Full range		−4.5		
				25°C		−5.3	−9	
R _{ref}	Reference resistance			Full range		1.25	6	kΩ
				25°C		1.4	2.3	
I _{CC}	Supply current		$\overline{\text{CS}}$, $\overline{\text{WR/RDY}}$, and $\overline{\text{RD}}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C _i	Input capacitance	D0–D7		Full range		5		pF
		ANLG IN				45		
C _O	Output capacitance	D0–D7		Full range			5	pF

† Full range is as specified in recommended operating conditions.



TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

operating characteristics, $V_{CC} = 5\text{ V}$, $V_{ref+} = 5\text{ V}$, $V_{ref-} = 0$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
kSVS	Supply-voltage sensitivity	V _{CC} = 5 V ± 5%, T _A = MIN to MAX		± 1/16		± 1/4	LSB
	Total unadjusted error‡	MODE at 0 V, T _A = MIN to MAX				1	LSB
t _{conv(R)}	Conversion time, read mode	MODE at 0 V,	See Figure 1	1.6		2.5	μs
t _{a(R)}	Access time, RD↓ to data valid	MODE at 0 V,	See Figure 1	t _{conv(R)} +20		t _{conv(R)} +50	ns
t _{a(R1)}	Access time, RD↓ to data valid	MODE at 5 V, t _{d(WR)} < t _{d(int)} , See Figure 2	C _L = 15 pF	190		280	ns
			C _L = 100 pF	210		320	
t _{a(R2)}	Access time, RD↓ to data valid	MODE at 5 V, t _{d(WR)} > t _{d(int)} , See Figure 3	C _L = 15 pF	70		120	ns
			C _L = 100 pF	90		150	
t _{a(INT)}	Access time, INT↓ to data valid	MODE at 5 V,	See Figure 4	20		50	ns
t _{dis}	Disable time, RD↑ to data valid	R _L = 1 kΩ, C _L = 10 pF, See Figures 1, 2, 3, and 5		70		95	ns
t _{d(int)}	Delay time, WR/RDY↑ to INT↓	MODE at 5 V, C _L = 50 pF, See Figures 2, 3, and 4		800		1300	ns
t _{d(NC)}	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500			ns
t _{d(WR)}	Delay time, WR/RDY↑ to RD↓ in write-read mode	See Figure 2		0.4			μs
t _{d(RDY)}	Delay time, CS↓ to WR/RDY↓	MODE at 0 V, See Figure 1	C _L = 50 pF,	50		100	ns
t _{d(RIH)}	Delay time, RD↑ to INT↑	C _L = 50 pF, See Figures 1, 2, and 3		125		225	ns
t _{d(RIL)}	Delay time, RD↓ to INT↓	MODE at 5 V, See Figure 2	t _{d(WR)} < t _{d(int)} ,	200		290	ns
t _{d(WIH)}	Delay time, WR/RDY↑ to INT↑	MODE at 5 V, See Figure 4	C _L = 50 pF,	175		270	ns
	Slew-rate tracking			0.1			V/μs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

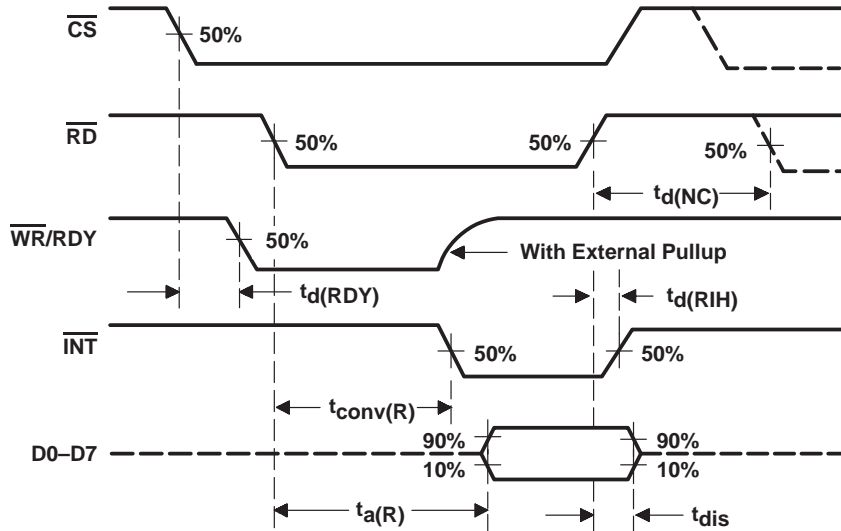


Figure 1. Read-Mode Waveforms (MODE Low)

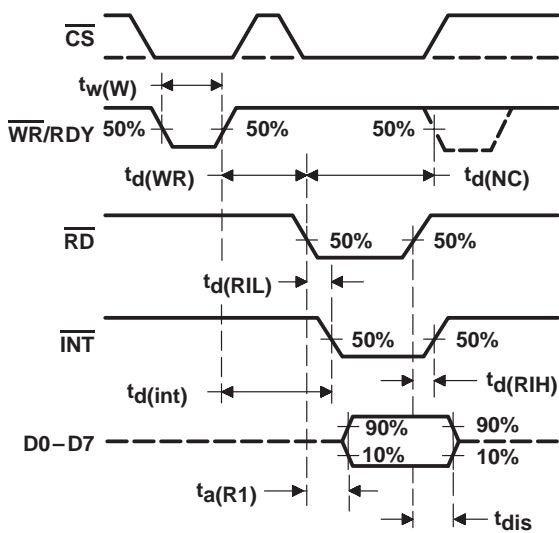


Figure 2. Write-Read-Mode Waveforms
[MODE High and $t_d(WR) < t_d(int)$]

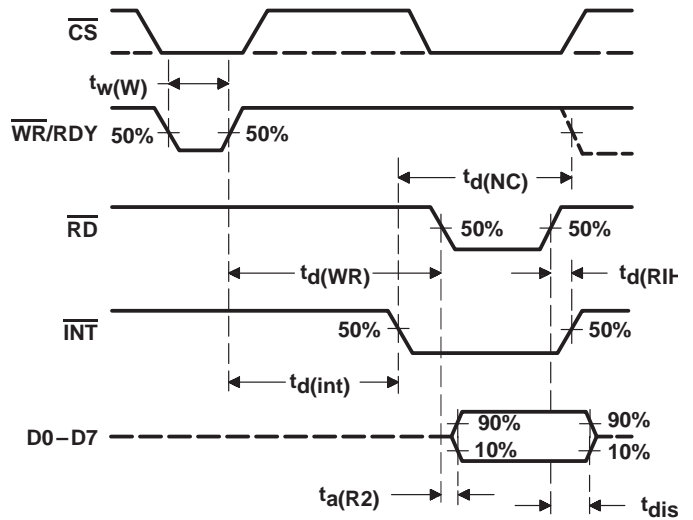


Figure 3. Write-Read-Mode Waveforms
[MODE High and $t_d(WR) > t_d(int)$]

TLC0820AC, TLC0820AI

Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

PARAMETER MEASUREMENT INFORMATION

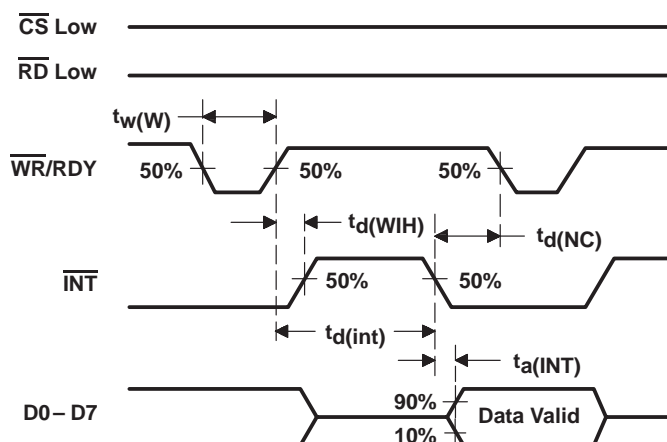
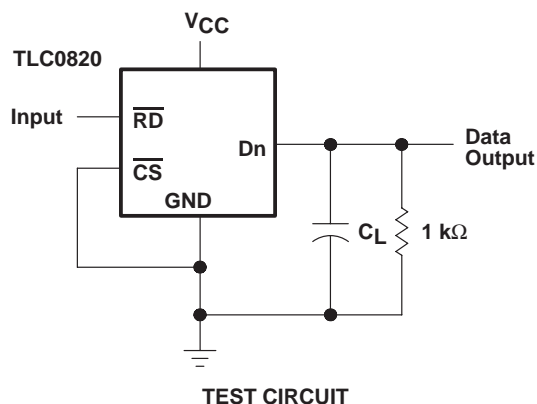
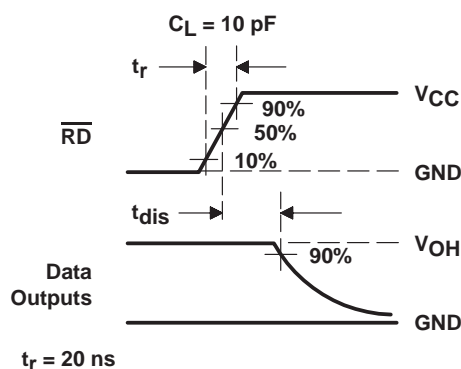


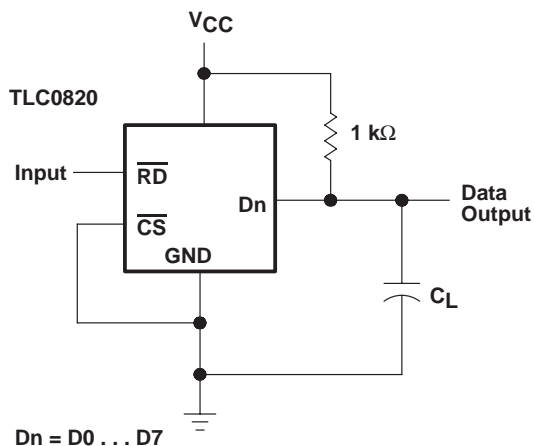
Figure 4. Write-Read-Mode Waveforms
(Stand-Alone Operation, MODE High, and \overline{RD} Low)



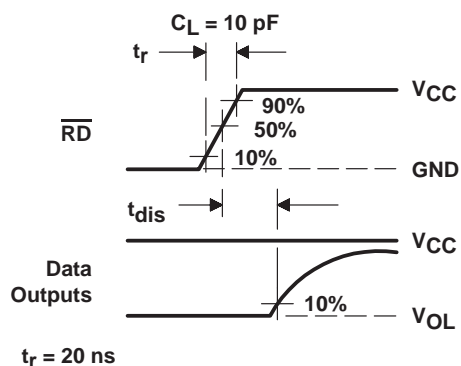
TEST CIRCUIT



VOLTAGE WAVEFORMS



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Test Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

The TLC0820AC and TLC0820AI each employ a combination of sampled-data comparator techniques and flash techniques common to many high-speed converters. Two 4-bit flash analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC} + 0.1\text{ V}$. Analog input signals that are less than $V_{ref-} + 1/2\text{ LSB}$ or greater than $V_{ref+} - 1/2\text{ LSB}$ convert to 00000000 or 11111111, respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{ref+} and V_{ref-} voltages.

The device operates in two modes, read (only) and write-read, that are selected by MODE. The converter is set to the read (only) mode when MODE is low. In the read mode, \overline{WR}/RDY is used as an output and is referred to as the ready terminal. In this mode, a low on \overline{WR}/RDY while \overline{CS} is low indicates that the device is busy. Conversion starts on the falling edge of \overline{RD} and is completed no more than $2.5\text{ }\mu\text{s}$ later when \overline{INT} falls and \overline{WR}/RDY returns to the high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, \overline{RD} is taken high, \overline{INT} returns high, and the data outputs return to their high-impedance states.

When MODE is high, the converter is set to the write-read mode and \overline{WR}/RDY is referred to as the write terminal. Taking \overline{CS} and \overline{WR}/RDY low selects the converter and initiates measurement of the input signal. Approximately 600 ns after \overline{WR}/RDY returns high, the conversion is completed. Conversion starts on the rising edge of \overline{WR}/RDY in the write-read mode.

The high-order 4-bit flash ADC measures the input by means of 16 comparators operating simultaneously. A high-precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the 3-state output buffers on the falling edge of \overline{RD} .

TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES

SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

APPLICATION INFORMATION

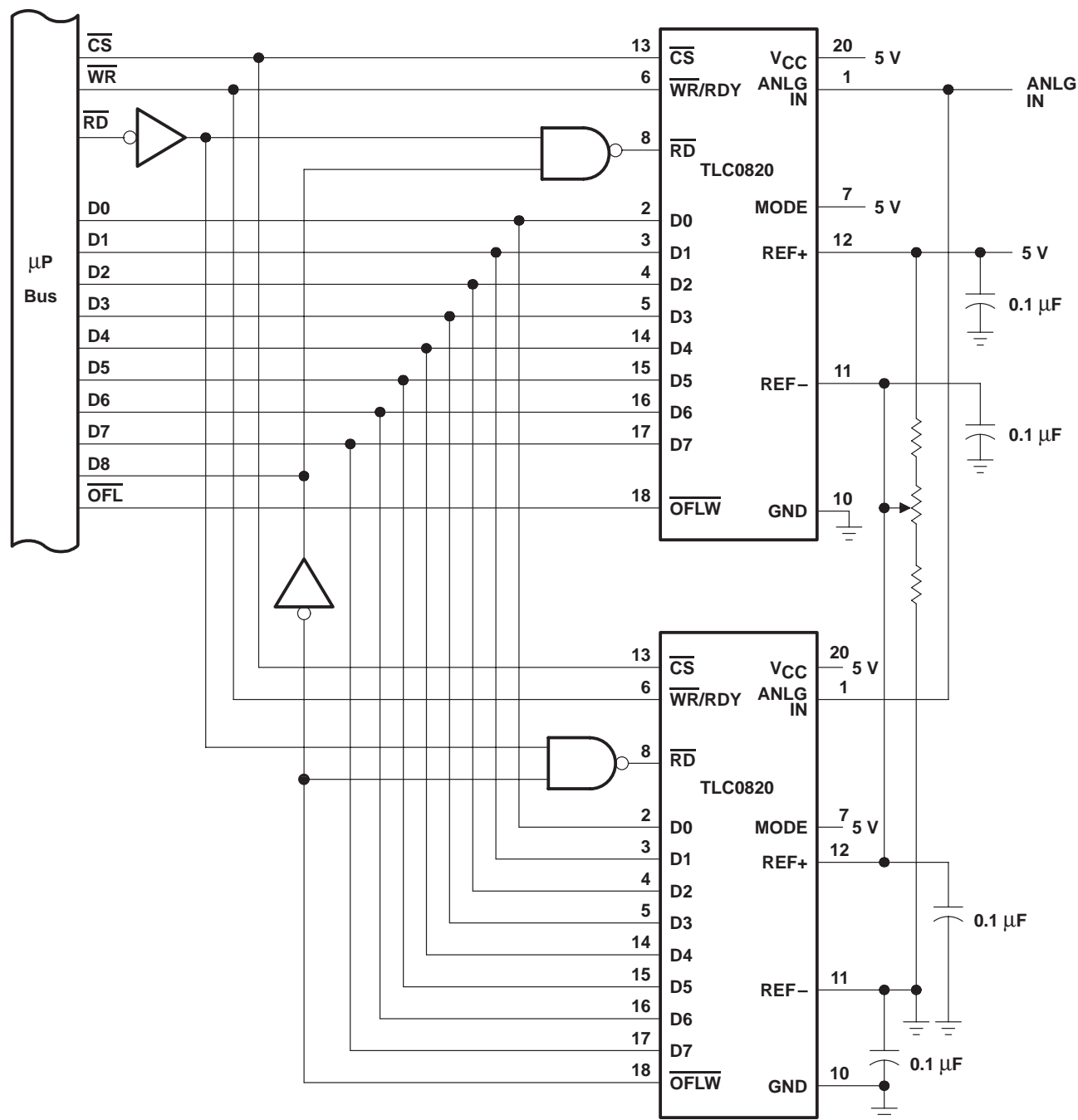


Figure 6. Configuration for 9-Bit Resolution

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC0820ACDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820ACNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820AIDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820AIFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820AIN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820AINE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC0820ACDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC0820ACDBR	SSOP	DB	20	2000	346.0	346.0	33.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated