

16-Bit, 8-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- BIPOLAR INPUT RANGE
- PIN-FOR-PIN COMPATIBLE WITH THE ADS7844 AND ADS8344
- SINGLE SUPPLY: 2.7V to 5V
- 8-CHANNEL SINGLE-ENDED OR 4-CHANNEL DIFFERENTIAL INPUT
- UP TO 100kHz CONVERSION RATE
- 85dB SINAD
- SERIAL INTERFACE
- QSOP-20 AND SSOP-20 PACKAGES

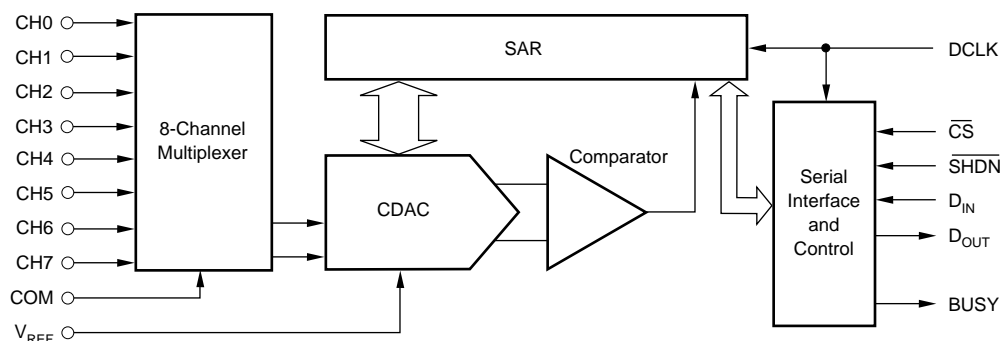
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS8345 is an 8-channel, 16-bit, sampling Analog-to-Digital (A/D) converter with a synchronous serial interface. Typical power dissipation is 8mW at a 100kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 500mV and $V_{CC}/2$, providing a corresponding input voltage range of $\pm V_{REF}$. The device includes a shutdown mode which reduces power dissipation to under 15 μ W. The ADS8345 is ensured down to 2.7V operation.

Low-power, high-speed, and an onboard multiplexer make the ADS8345 ideal for battery-operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS8345 is available in a QSOP-20 or SSOP-20 package and is ensured over the -40°C to $+85^{\circ}\text{C}$ temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|-------------------------------------|
| +V _{CC} to GND | –0.3V to +6V |
| Analog Inputs to GND | –0.3V to (+V _{CC}) + 0.3V |
| Digital Inputs to GND | –0.3V to +6V |
| Power Dissipation | 250mW |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

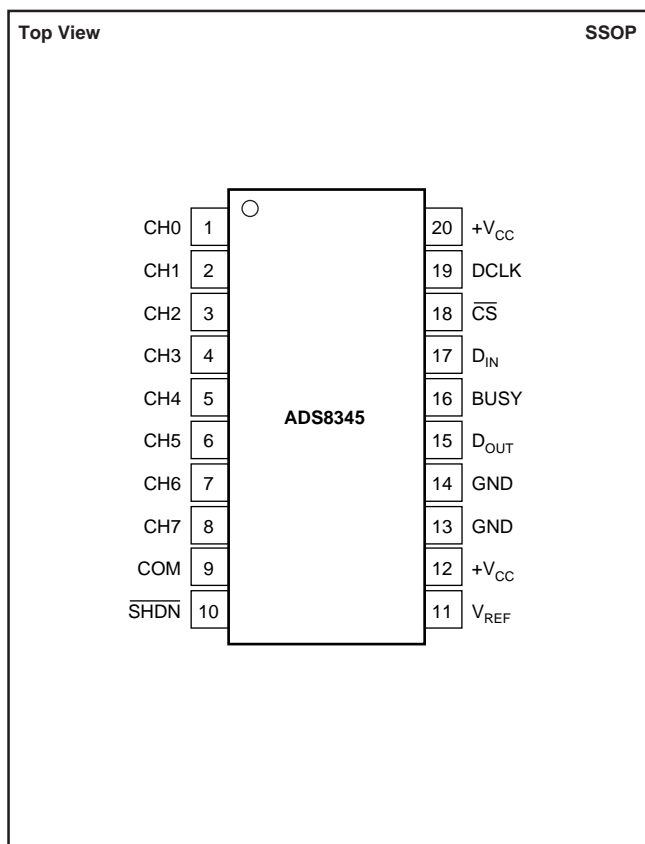
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MAXIMUM GAIN ERROR (%) | PACKAGE-LEAD | PACKAGE DESIGNATOR ⁽¹⁾ | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|-----------|--|------------------------|--------------|-----------------------------------|-----------------------------|-----------------|---------------------------|
| ADS8345E | 8 | ±0.05 | QSOP-20 | DBQ | –40°C to +85°C | ADS8345E | Rails, 100 |
| " | " | " | " | " | " | ADS8345E/2K5 | Tape and Reel, 2500 |
| ADS8345N | 8 | ±0.05 | SSOP-20 | DB | –40°C to +85°C | ADS8345N | Rails, 100 |
| " | " | " | " | " | " | ADS8345N/1K | Tape and Reel, 1000 |
| ADS8345EB | 6 | ±0.024 | QSOP-20 | DBQ | –40°C to +85°C | ADS8345EB | Rails, 100 |
| " | " | " | " | " | " | ADS8345EB/2K5 | Tape and Reel, 2500 |
| ADS8345NB | 6 | ±0.024 | SSOP-20 | DB | –40°C to +85°C | ADS8345NB | Rails, 100 |
| " | " | " | " | " | " | ADS8345NB/1K | Tape and Reel, 1000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION



PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|-----|------------------|---|
| 1 | CH0 | Analog Input Channel 0 |
| 2 | CH1 | Analog Input Channel 1 |
| 3 | CH2 | Analog Input Channel 2 |
| 4 | CH3 | Analog Input Channel 3 |
| 5 | CH4 | Analog Input Channel 4 |
| 6 | CH5 | Analog Input Channel 5 |
| 7 | CH6 | Analog Input Channel 6 |
| 8 | CH7 | Analog Input Channel 7 |
| 9 | COM | Common reference for analog inputs. This pin is typically connected to V _{REF} . |
| 10 | SHDN | Shutdown. When LOW, the device enters a very low-power shutdown mode. |
| 11 | V _{REF} | Voltage Reference Input. See the Electrical Characteristics Table for ranges. |
| 12 | +V _{CC} | Power Supply, 2.7V to 5.25V |
| 13 | GND | Ground |
| 14 | GND | Ground |
| 15 | D _{OUT} | Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH. |
| 16 | BUSY | Busy Output. Busy goes LOW when the D _{IN} control bits are being read and also when the device is converting. The Output is high impedance when CS is HIGH. |
| 17 | D _{IN} | Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK. |
| 18 | CS | Chip Select Input; Active LOW. Data will not be clocked into D _{IN} unless CS is LOW. When CS is HIGH, D _{OUT} is high impedance. |
| 19 | DCLK | External Clock Input. The clock speed determines the conversion rate by the equation $f_{DCLK} = 24 \cdot f_{SAMPLE}$. |
| 20 | +V _{CC} | Power Supply |

ELECTRICAL CHARACTERISTICS: +5V

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{CC} = +5\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{CLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS8345E, N | | | ADS8345EB, NB | | | UNITS |
|--|---|-------------------------|---------|-----------------|---------------|-----|-------------|--------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | 16 | | | * | | Bits |
| ANALOG INPUT | | | | | | | | |
| Full-Scale Input Span | Positive Input-Negative Input | $-V_{REF}$ | | $+V_{REF}$ | * | | * | V |
| Absolute Input Range | +IN | -0.2 | | $+V_{CC} + 0.2$ | * | | * | V |
| | -IN | -0.2 | | $+V_{CC} + 0.2$ | * | | * | V |
| Capacitance | | | 25 | | | * | | pF |
| Leakage Current | | | ± 1 | | | * | | μA |
| SYSTEM PERFORMANCE | | | | | | | | |
| No Missing Codes | | 14 | | | 15 | | | Bits |
| Integral Linearity Error | | | | ± 8 | | | ± 6 | LSB |
| Bipolar Error | | | | ± 2 | | | ± 1 | mV |
| Bipolar Error Match | | | 4 | 8 | * | | * | LSB ⁽¹⁾ |
| Gain Error | | | | ± 0.05 | | | ± 0.024 | % |
| Gain Error Match | | | 1.0 | 4 | * | | * | LSB |
| Noise | | | 20 | | * | | * | μVrms |
| Power-Supply Rejection | $+4.75\text{V} < V_{CC} < 5.25\text{V}$ | | 3 | | * | | * | LSB ⁽¹⁾ |
| SAMPLING DYNAMICS | | | | | | | | |
| Conversion Time | | | | 16 | | | * | CLK Cycles |
| Acquisition Time | | 4.5 | | | * | | * | CLK Cycles |
| Throughput Rate | | | | 100 | | | * | kHz |
| Multiplexer Settling Time | | | 500 | | | * | | ns |
| Aperture Delay | | | 30 | | | * | | ns |
| Aperture Jitter | | | 100 | | | * | | ps |
| Internal Clock Frequency | $\overline{\text{SHDN}} = V_{DD}$ | | 2.4 | | | * | | MHz |
| External Clock Frequency | | 0.024 | | 2.4 | * | | * | MHz |
| | Data Transfer Only | 0 | | 2.4 | * | | * | MHz |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| Total Harmonic Distortion ⁽²⁾ | $V_{IN} = 5\text{Vp-p}$ at 10kHz | | -96 | | | * | | dB |
| Signal-to-(Noise + Distortion) | $V_{IN} = 5\text{Vp-p}$ at 10kHz | | 85 | | | * | | dB |
| Spurious-Free Dynamic Range | $V_{IN} = 5\text{Vp-p}$ at 10kHz | | 98 | | | * | | dB |
| Channel-to-Channel Isolation | $V_{IN} = 5\text{Vp-p}$ at 10kHz | | 105 | | | * | | dB |
| REFERENCE INPUT | | | | | | | | |
| Range | | 0.5 | | $+V_{CC}/2$ | * | | * | V |
| Resistance | DCLK Static | | 5 | | | * | * | $\text{G}\Omega$ |
| Input Current | | | 40 | 100 | | * | * | μA |
| | DCLK Static | | 0.001 | 3 | | * | * | μA |
| DIGITAL INPUT/OUTPUT | | | | | | | | |
| Logic Family | | | CMOS | | | * | | |
| Logic Levels | | | | | | | | |
| V_{IH} | $ I_{IH} \leq +5\mu\text{A}$ | 3.0 | | 5.5 | * | | * | V |
| V_{IL} | $ I_{IL} \leq +5\mu\text{A}$ | -0.3 | | +0.8 | * | | * | V |
| V_{OH} | $I_{OH} = -250\mu\text{A}$ | 3.5 | | | * | | * | V |
| V_{OL} | $I_{OL} = 250\mu\text{A}$ | | | 0.4 | | | * | V |
| Data Format | | Binary Two's Complement | | | | * | | |
| POWER-SUPPLY REQUIREMENTS | | | | | | | | |
| $+V_{CC}$ | Specified Performance | 4.75 | | 5.25 | * | | * | V |
| Quiescent Current | | | 1.5 | 2.0 | | * | * | mA |
| | $f_{\text{SAMPLE}} = 10\text{kHz}$ | | 1.2 | | | * | * | mA |
| | Power-Down Mode ⁽³⁾ , $\overline{\text{CS}} = +V_{CC}$ | | | 3 | | * | * | μA |
| Power Dissipation | | | 7.5 | 10 | | * | * | mW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | $^{\circ}\text{C}$ |

* Same specifications as ADS8345E, N.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 76 μV . (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{\text{SHDN}} = \text{GND}$.

ELECTRICAL CHARACTERISTICS: +2.7V

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +1.25\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{CLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.

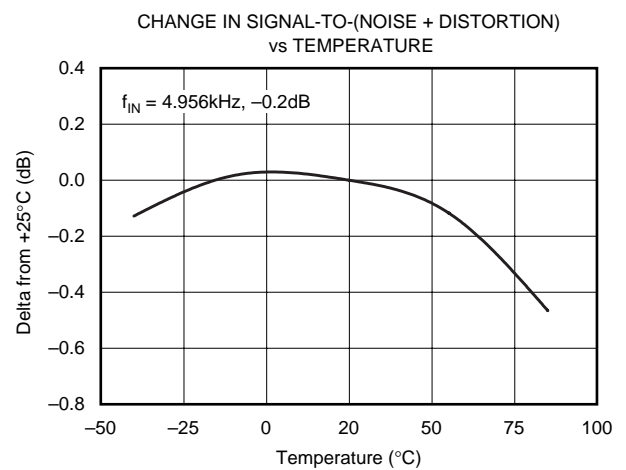
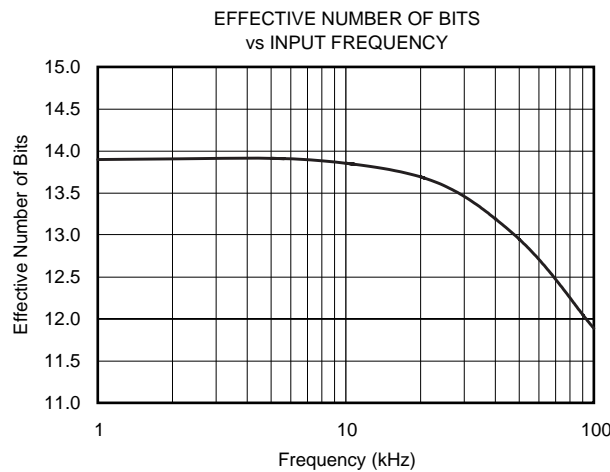
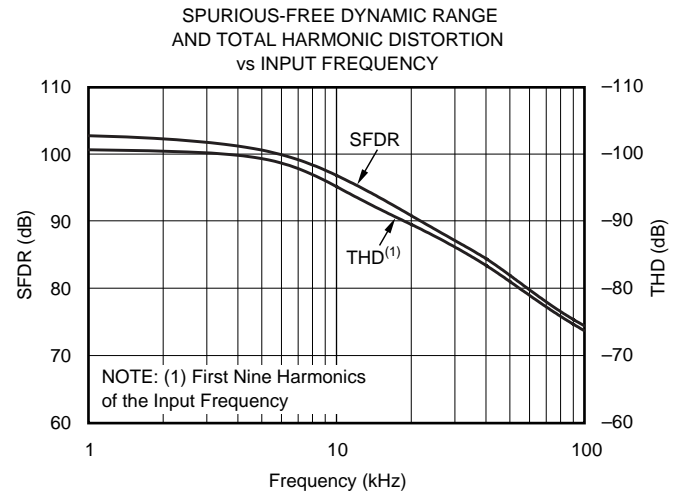
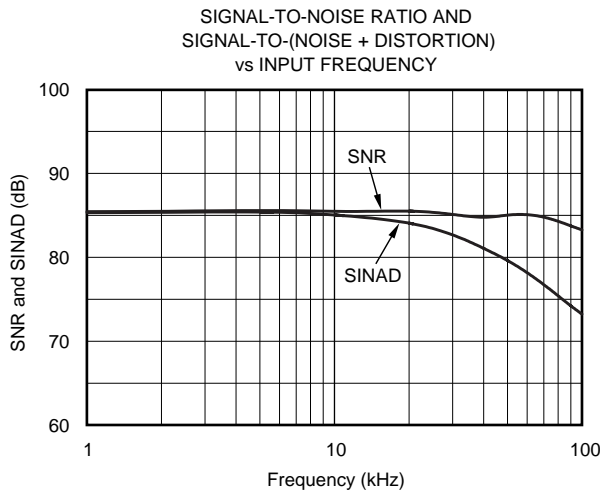
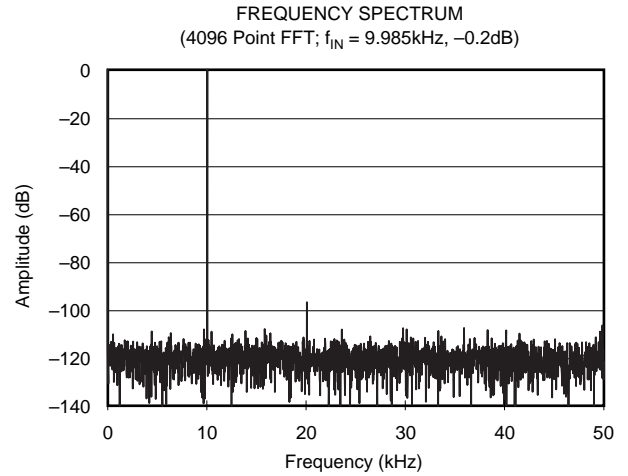
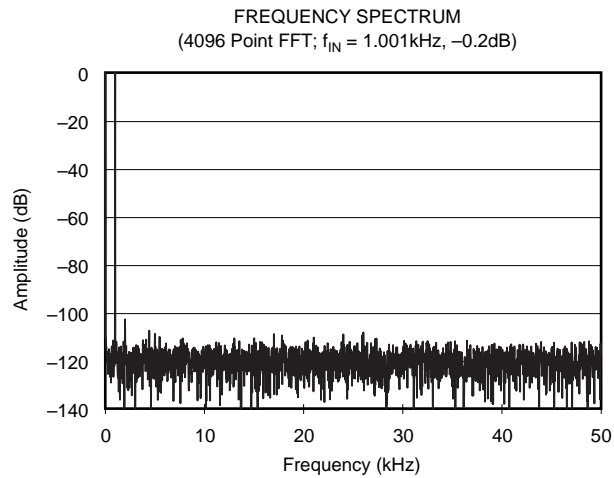
| PARAMETER | CONDITIONS | ADS8345E, N | | | ADS8345EB, NB | | | UNITS |
|--|---|---------------------|-------------------------|-----------------|---------------|-----|-------------|----------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | 16 | | | * | | Bits |
| ANALOG INPUT | | | | | | | | |
| Full-Scale Input Span | Positive Input-Negative Input | $-V_{REF}$ | | $+V_{REF}$ | * | | * | V |
| Absolute Input Range | +IN | -0.2 | | $+V_{CC} + 0.2$ | * | | * | V |
| | -IN | -0.2 | | $+V_{CC} + 0.2$ | * | | * | V |
| Capacitance | | | 25 | | | * | | pF |
| Leakage Current | | | ± 1 | | | * | | μA |
| SYSTEM PERFORMANCE | | | | | | | | |
| No Missing Codes | | 14 | | | 15 | | | Bits |
| Integral Linearity Error | | | | ± 8 | | | ± 6 | LSB |
| Bipolar Error | | | | ± 1.0 | | | ± 0.5 | mV |
| Bipolar Error Match | | | 2 | 4 | | * | * | LSB |
| Gain Error | | | | ± 0.05 | | | ± 0.024 | % of FSR |
| Gain Error Match | | | 1 | 4 | | * | * | LSB |
| Noise | | | 20 | | | * | * | μV_{rms} |
| Power-Supply Rejection | $+2.7 < V_{CC} < +3.3\text{V}$ | | 3 | | | * | * | LSB ⁽¹⁾ |
| SAMPLING DYNAMICS | | | | | | | | |
| Conversion Time | | 4.5 | | 16 | * | | * | CLK Cycles |
| Acquisition Time | | | | | | | | CLK Cycles |
| Throughput Rate | | | | 100 | | | * | kHz |
| Multiplexer Settling Time | | | 500 | | | * | | ns |
| Aperture Delay | | | 30 | | | * | | ns |
| Aperture Jitter | | | 100 | | | * | | ps |
| Internal Clock Frequency | $\overline{\text{SHDN}} = V_{DD}$ | | 2.4 | | | * | | MHz |
| External Clock Frequency | | 0.024 | | 2.4 | * | | * | MHz |
| | When used with Internal Clock | 0.024 | | 2.0 | * | | * | MHz |
| | Data Transfer Only | 0 | | 2.4 | * | | * | MHz |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| Total Harmonic Distortion ⁽²⁾ | $V_{IN} = 2.5\text{Vp-p}$ at 1kHz | | -95 | | | * | | dB |
| Signal-to-(Noise + Distortion) | $V_{IN} = 2.5\text{Vp-p}$ at 1kHz | | 81 | | | * | | dB |
| Spurious-Free Dynamic Range | $V_{IN} = 2.5\text{Vp-p}$ at 1kHz | | 95 | | | * | | dB |
| Channel-to-Channel Isolation | $V_{IN} = 2.5\text{Vp-p}$ at 10kHz | | 108 | | | * | | dB |
| REFERENCE INPUT | | | | | | | | |
| Range | | 0.5 | | $+V_{CC}/2$ | * | | * | V |
| Resistance | DCLK Static | | 5 | | | * | | $\text{G}\Omega$ |
| Input Current | | | 13 | 40 | | * | * | μA |
| | DCLK Static | | 0.001 | 3 | | * | * | μA |
| DIGITAL INPUT/OUTPUT | | | | | | | | |
| Logic Family | | | CMOS | | | * | | |
| Logic Levels | | | | | | | | |
| V_{IH} | $ I_{IH} \leq +5\mu\text{A}$ | $+V_{CC} \cdot 0.7$ | | 5.5 | * | | * | V |
| V_{IL} | $ I_{IL} \leq +5\mu\text{A}$ | -0.3 | | +0.8 | * | | * | V |
| V_{OH} | $I_{OH} = -250\mu\text{A}$ | $+V_{CC} \cdot 0.8$ | | | * | | * | V |
| V_{OL} | $I_{OL} = 250\mu\text{A}$ | | | 0.4 | | | * | V |
| Data Format | | | Binary Two's Complement | | | * | | |
| POWER-SUPPLY REQUIREMENTS | | | | | | | | |
| $+V_{CC}$ | Specified Performance | 2.7 | | 3.6 | * | | * | V |
| Quiescent Current | | | 1.2 | 1.85 | | * | * | mA |
| | $f_{\text{SAMPLE}} = 10\text{kHz}$ | | 950 | | | * | * | μA |
| | Power-Down Mode ⁽³⁾ , $\overline{\text{CS}} = +V_{CC}$ | | | 3 | | * | * | μA |
| Power Dissipation | | | 3.2 | 5 | | * | * | mW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | $^{\circ}\text{C}$ |

* Same specifications as ADS8345E, N.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +1.25V, one LSB is 38 μV . (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{\text{SHDN}} = \text{GND}$.

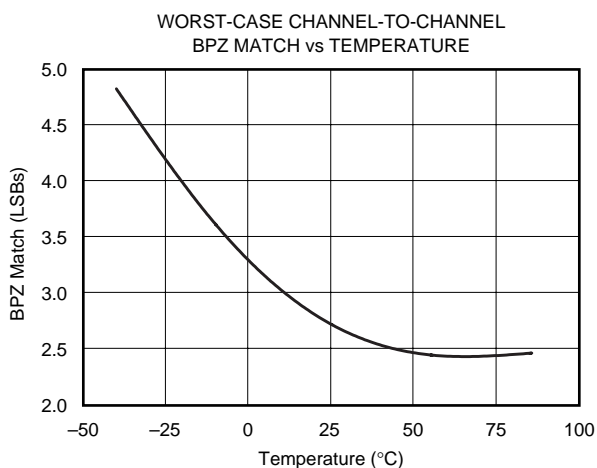
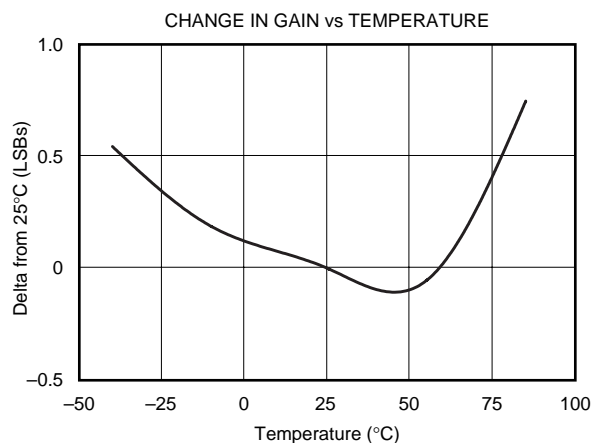
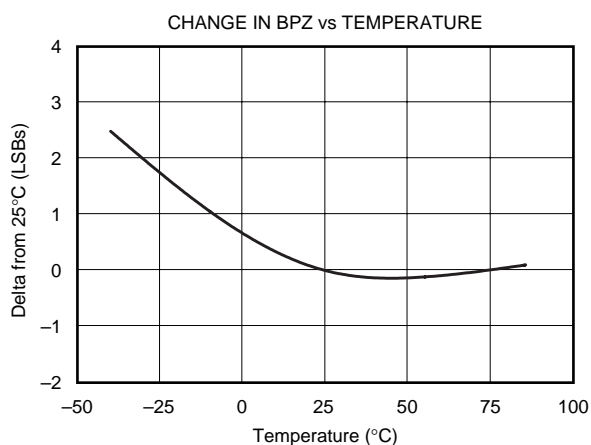
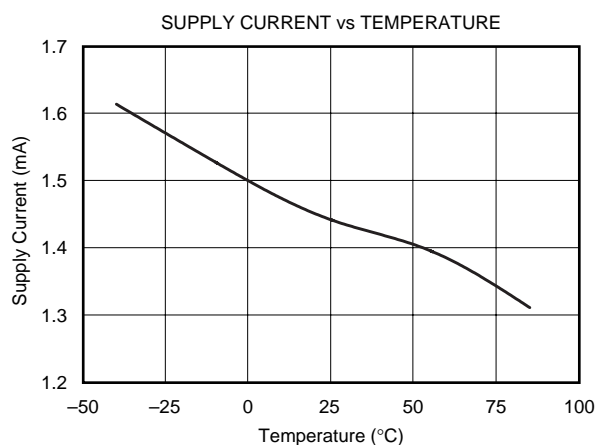
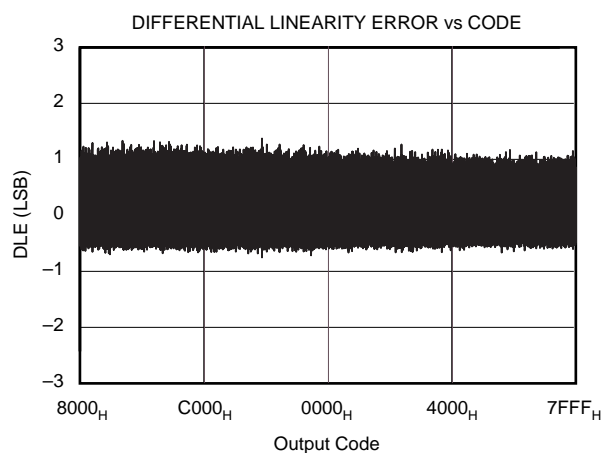
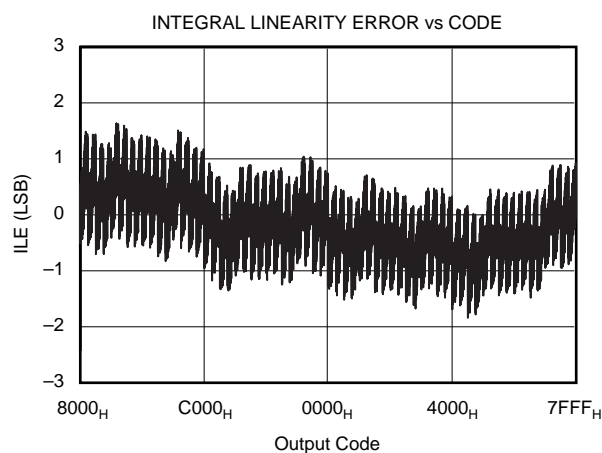
TYPICAL CHARACTERISTICS: +5V

At $T_A = +25^\circ\text{C}$, $+V_{CC} = +5\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{DCLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.



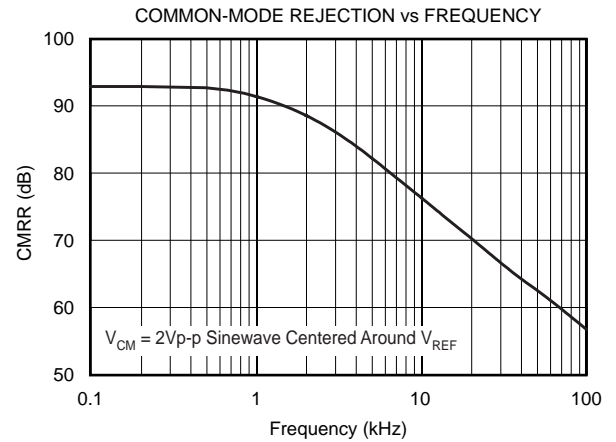
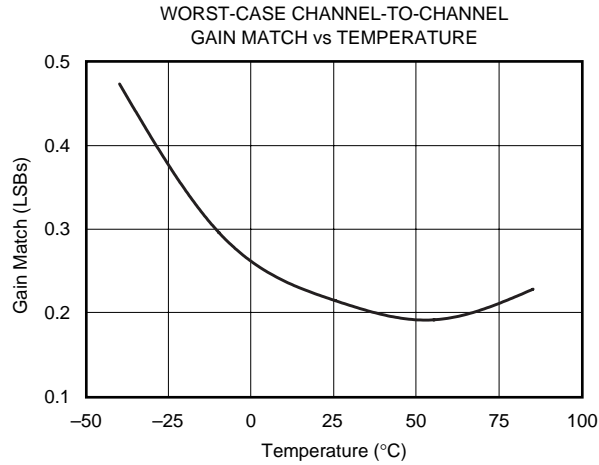
TYPICAL CHARACTERISTICS: +5V (Cont.)

At $T_A = +25^\circ\text{C}$, $V_{CC} = +5\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{DCLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.



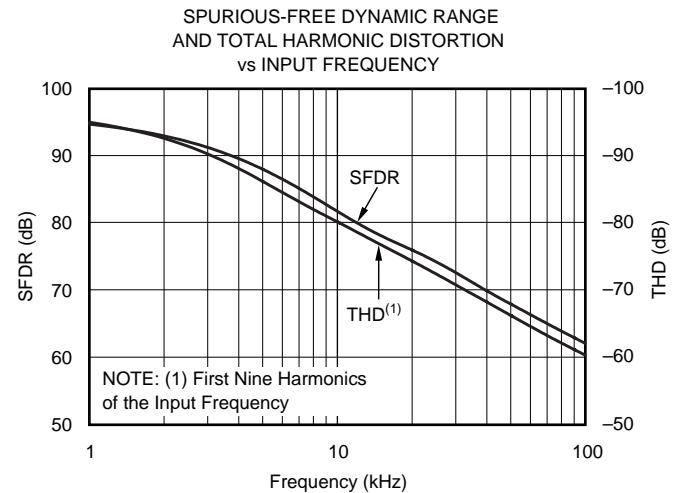
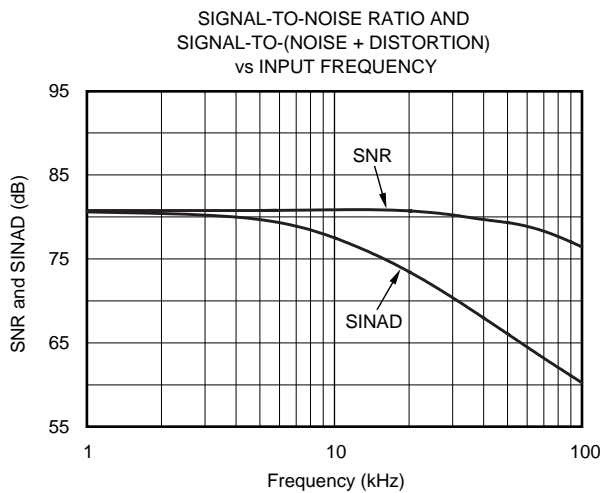
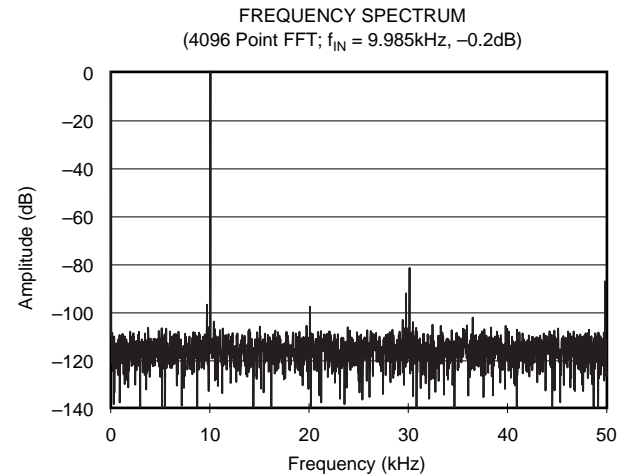
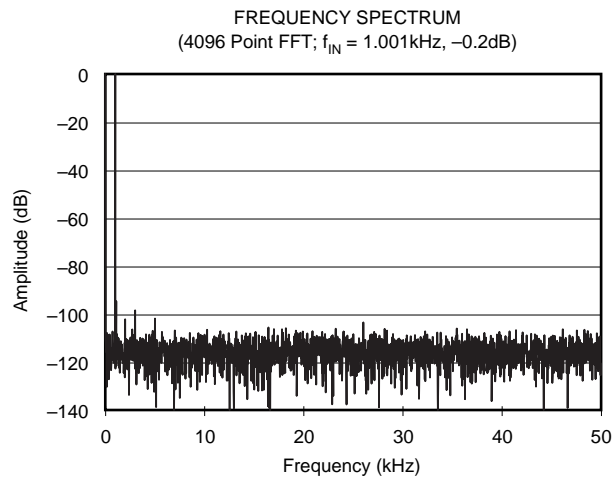
TYPICAL CHARACTERISTICS: +5V (Cont.)

At $T_A = +25^\circ\text{C}$, $+V_{CC} = +2.5\text{V}$, $V_{REF} = +2.5\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{DCLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.



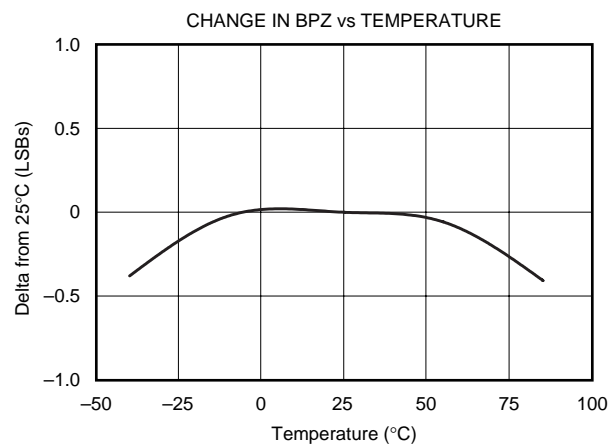
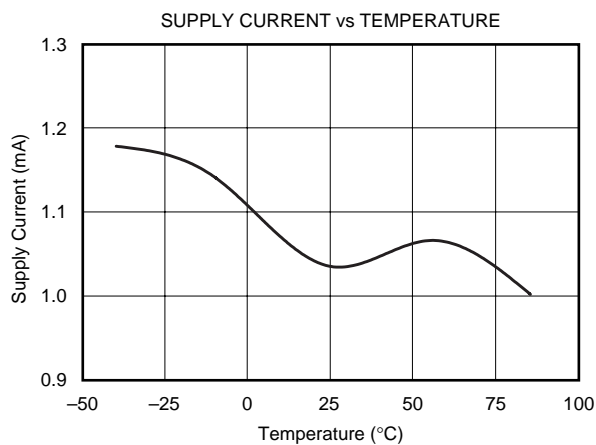
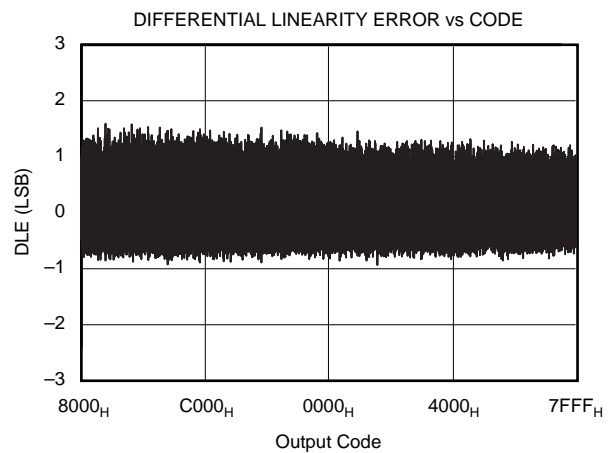
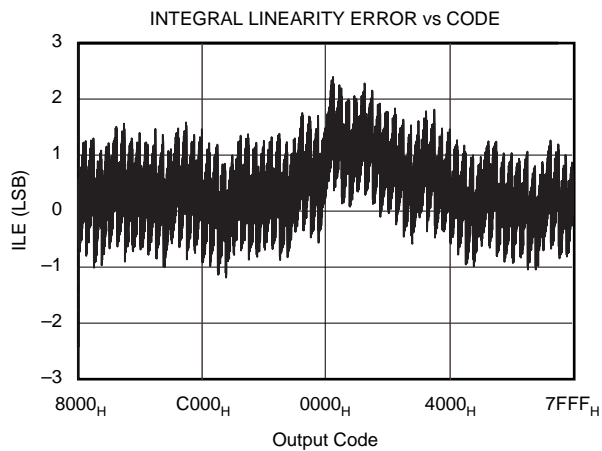
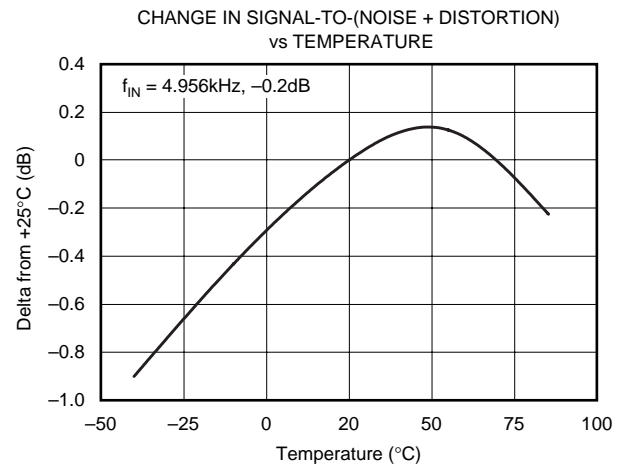
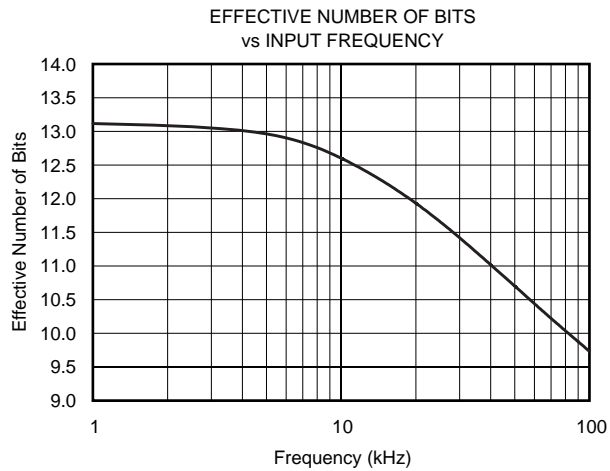
TYPICAL CHARACTERISTICS: +2.7V

At $T_A = +25^\circ\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +1.25\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{DCLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.



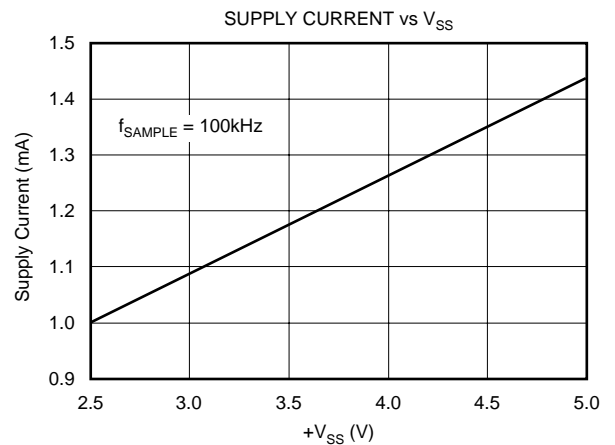
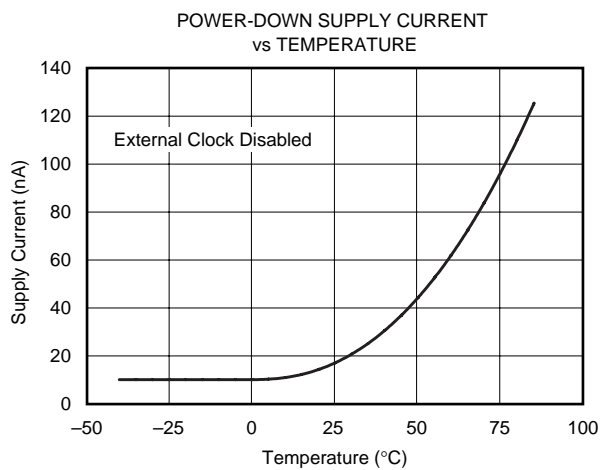
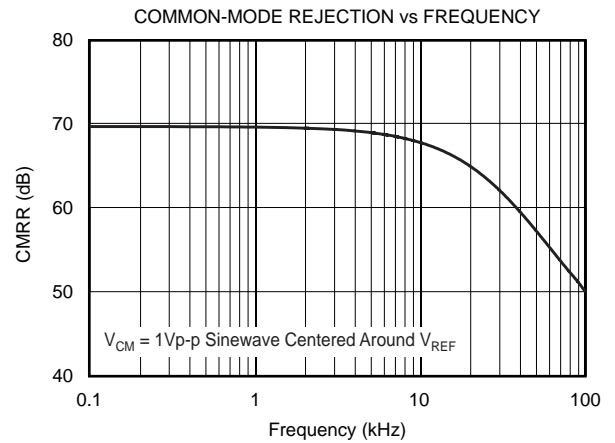
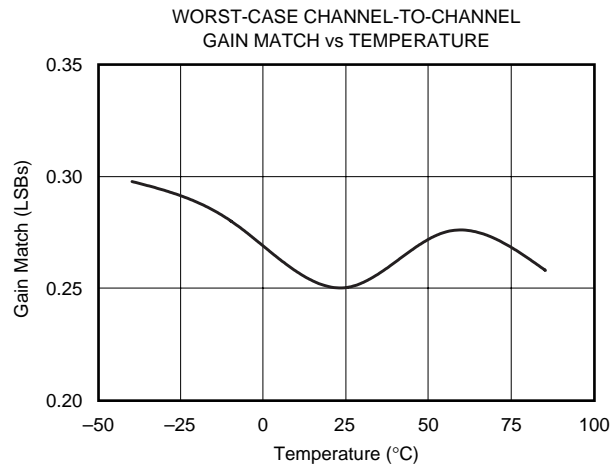
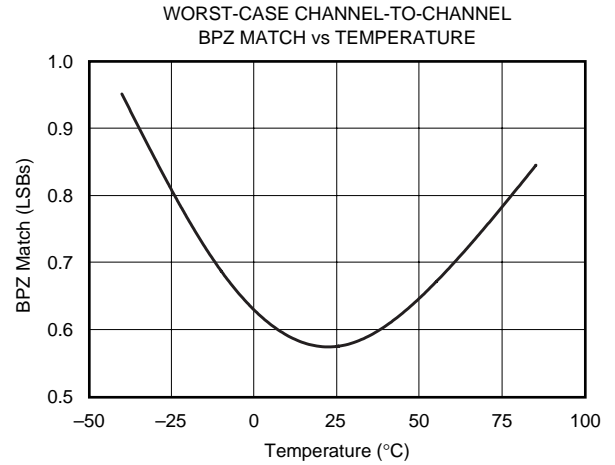
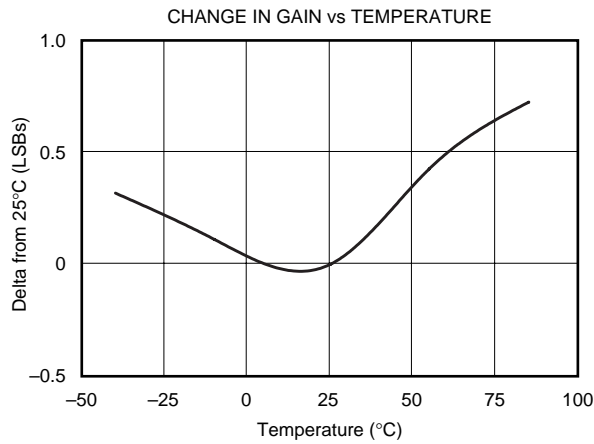
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At $T_A = +25^\circ\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +1.25\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, and $f_{\text{DCLK}} = 24 \cdot f_{\text{SAMPLE}} = 2.4\text{MHz}$, unless otherwise noted.



TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At $T_A = +25^\circ\text{C}$, $+V_{CC} = +2.7\text{V}$, $V_{REF} = +1.25\text{V}$, $f_{SAMPLE} = 100\text{kHz}$, and $f_{DCLK} = 24 \cdot f_{SAMPLE} = 2.4\text{MHz}$, unless otherwise noted.



THEORY OF OPERATION

The ADS8345 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6μm CMOS process.

The basic operation of the ADS8345 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 500mV and $+V_{CC}/2$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS8345.

The analog input to the converter is differential and is provided via an eight-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally $+V_{CC}/2$) or differentially by using four of the eight input channels (CH-CH7). The particular configuration is selectable via the digital interface.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8345: single-ended or differential (see Figure 2). When the input is single-ended, the COM input is held at a fixed voltage. The CHX input swings around the same voltage and the peak-to-peak amplitude is $2 \cdot V_{REF}$. The value of V_{REF}

determines the range over which the common voltage may vary (see Figure 3).

When the input is differential, the amplitude of the input is the difference between the CHX and COM input (see Figure 4). A voltage or signal is common to both of these inputs. The peak-to-peak amplitude of each input is V_{REF} about this common voltage. However, since the input are 180°C out-of-phase, the peak-to-peak amplitude of the difference voltage is $2 \cdot V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 5).

In each case, care should be taken to ensure that the output impedance of the sources driving the CHX and COM inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which changes with both temperature and input voltage. If the impedance cannot be matched, the errors can be lessened by giving the ADS8345 additional acquisition time.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8345 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current.

Care must be taken regarding the absolute analog input voltage. Outside of these ranges, the converter's linearity may not meet specifications. Please refer to the Electrical Characteristics table for min/max ratings.

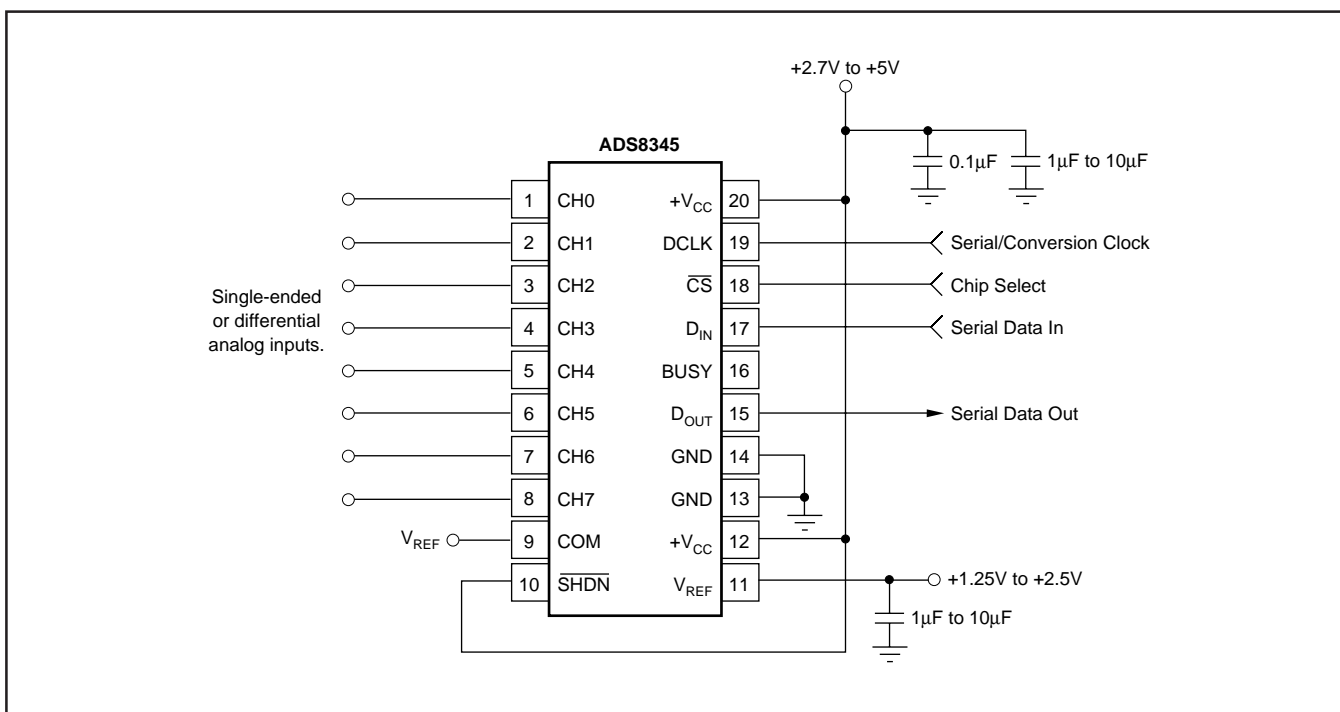


FIGURE 1. Basic Operation of the ADS8345.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8345 will operate with a reference in the range of 500mV to $+V_{CC}/2$. Keep in mind that the analog input is the differ-

ence between the CHX input and the COM input, as shown in Figure 4. For example, in the single-ended mode, a 1.25V reference with the COM pin at $V_{CC}/2$, the selected input channel (CH0-CH7) will properly digitize a signal in the range of $(V_{CC}/2 - 1.25V)$ to $(V_{CC}/2 + 1.25V)$.

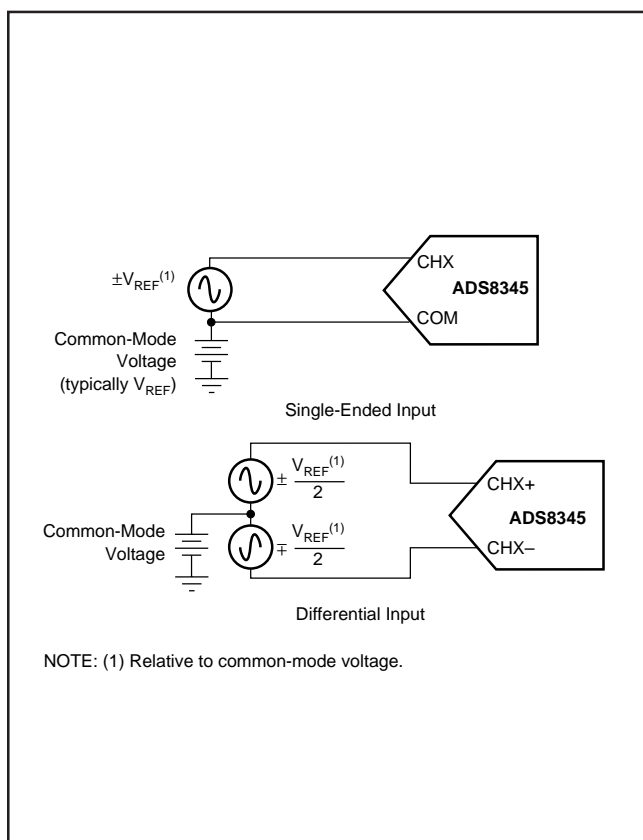


FIGURE 2. Methods of Driving the ADS8345—Single-Ended or Differential.

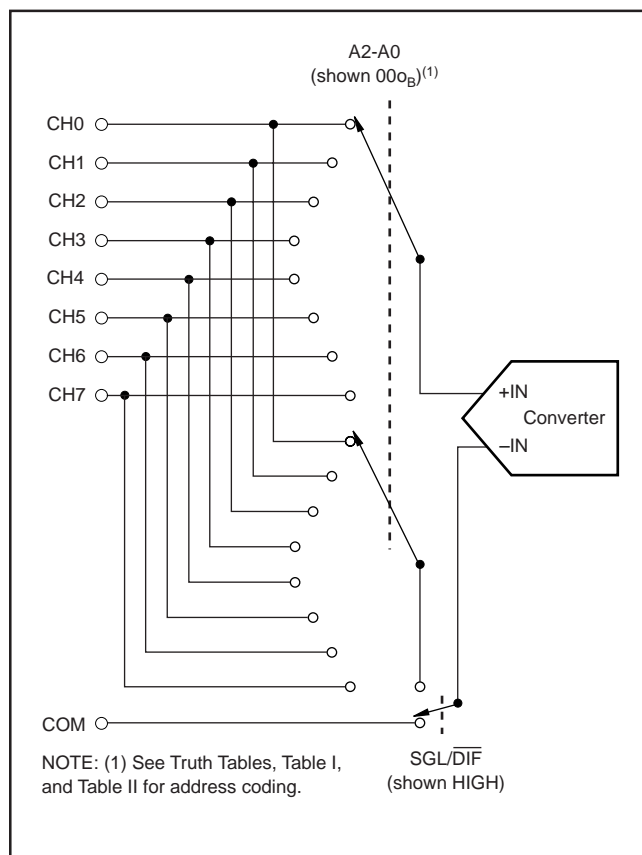


FIGURE 4. Simplified Diagram of the Analog Input.

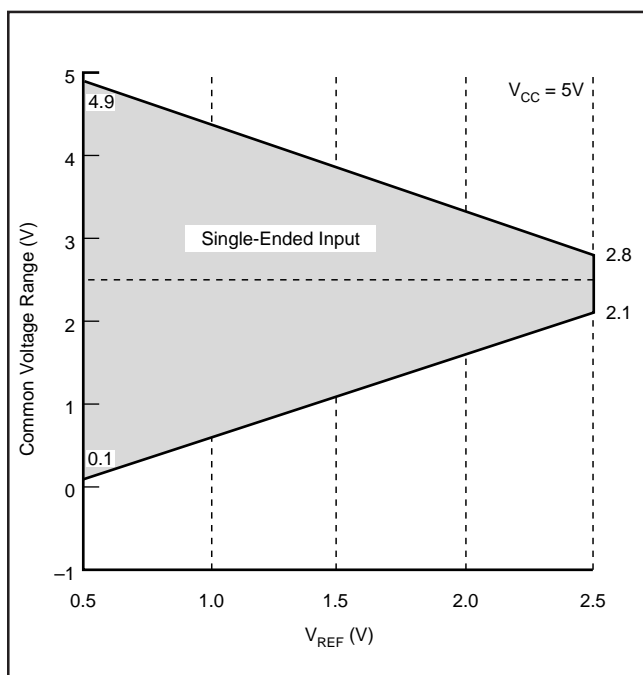


FIGURE 3. Single-Ended Input—Common Voltage Range vs V_{REF} .

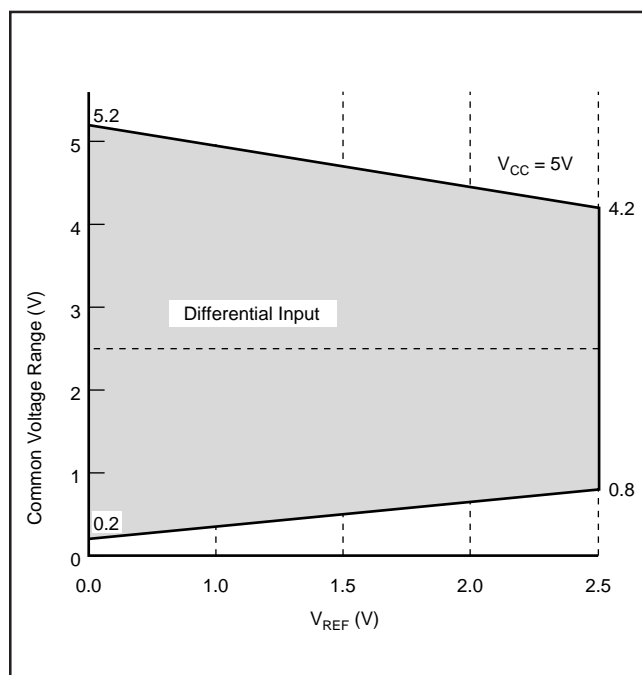


FIGURE 5. Differential Input—Common Voltage Range vs V_{REF} .

There are several critical items concerning the reference input and its wide-voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (Least Significant Bit) size and is equal to the reference voltage divided by 65536. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, then it will typically be 10LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 152.8 μ V.

The noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 500mV, the LSB size is 15.3 μ V. This level is below the internal noise of the device. As a result, the digital output code will not be stable and will vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS8345. Typically, the input current is 13 μ A with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

The ADS8345 has a 4-wire serial interface compatible with several microprocessor families (note that the digital inputs are over-voltage tolerant up to +5.5V, regardless of $+V_{CC}$). Figure 6 shows the typical operation of the ADS8345 digital interface.

Most microprocessors communicate using 8-bit transfers; the ADS8345 can complete a conversion with three such transfers, for a total of 24 clock cycles on the DCLK input, provided the timing is as shown in Figure 6.

The first eight clock cycles are used to provide the control byte via the D_{IN} pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After four more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the Hold mode. The next sixteen clock cycles accomplish the actual A/D conversion.

Control Byte

Figure 6 shows placement and order of the control bits within the control byte. Tables I and II give detailed information about these bits. The first bit, the "S" bit, must always be HIGH and indicates the start of the control byte. The ADS8345 will ignore inputs on the D_{IN} pin until the START bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Tables III and IV and Figure 4).

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|-------------|-------|-------|-------|-------|---------|-------|-------------|
| S | A2 | A1 | A0 | — | SGL/DIF | PD1 | PD0 |

TABLE I. Order of the Control Bits in the Control Byte.

| BIT | NAME | DESCRIPTION |
|-----|---------|--|
| 7 | S | Start Bit. Control byte starts with first HIGH bit on D_{IN} . |
| 6-4 | A2-A0 | Channel Select Bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input. |
| 2 | SGL/DIF | Single-Ended/Differential Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input. |
| 1-0 | PD1-PD0 | Power-Down Mode Select Bits. See Table V for details. |

TABLE II. Descriptions of the Control Bits within the Control Byte.

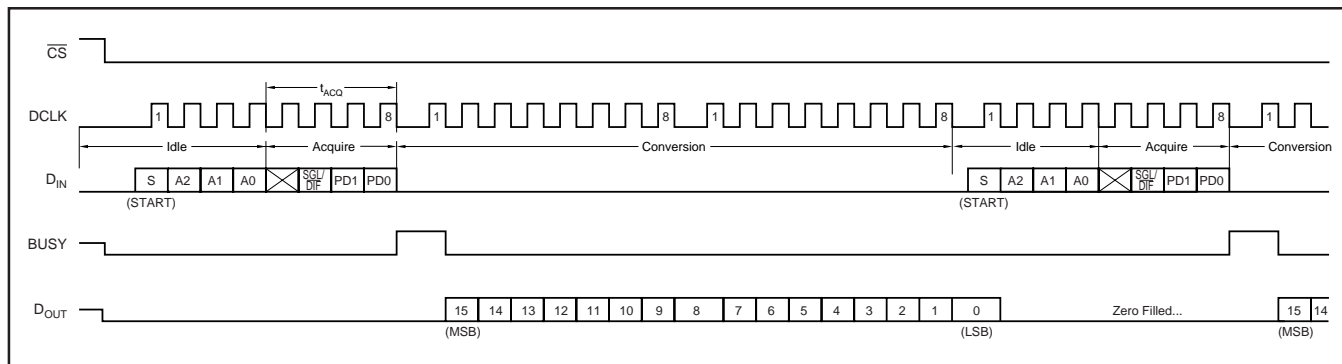


FIGURE 6. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

The SGL/DIF-bit controls the multiplexer input mode: either in single-ended mode, where the selected input channel is referenced to the COM pin, or in differential mode, where the two selected inputs provide a differential input. See Tables III and IV and Figure 4 for more information. The last two bits (PD1-PD0) select the Power-Down mode and Clock mode, as shown in Table V. If both PD1 and PD0 are HIGH, the device is always powered up. If both PD1 and PD0 are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

| A2 | A1 | A0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | COM |
|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | +IN | | | | | | | | -IN |
| 1 | 0 | 0 | | +IN | | | | | | | -IN |
| 0 | 0 | 1 | | | +IN | | | | | | -IN |
| 1 | 0 | 1 | | | | +IN | | | | | -IN |
| 0 | 1 | 0 | | | | | +IN | | | | -IN |
| 1 | 1 | 0 | | | | | | +IN | | | -IN |
| 0 | 1 | 1 | | | | | | | +IN | | -IN |
| 1 | 1 | 1 | | | | | | | | +IN | -IN |

TABLE III. Single-Ended Channel Selection (SGL/DIF HIGH).

| A2 | A1 | A0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 |
|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | +IN | -IN | | | | | | |
| 0 | 0 | 1 | | | +IN | -IN | | | | |
| 0 | 1 | 0 | | | | | +IN | -IN | | |
| 0 | 1 | 1 | | | | | | | +IN | -IN |
| 1 | 0 | 0 | -IN | +IN | | | | | | |
| 1 | 0 | 1 | | | -IN | +IN | | | | |
| 1 | 1 | 0 | | | | | -IN | +IN | | |
| 1 | 1 | 1 | | | | | | | -IN | +IN |

TABLE IV. Differential Channel Control (SGL/DIF LOW).

| PD1 | PD0 | DESCRIPTION |
|-----|-----|---|
| 0 | 0 | Power-down between conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. |
| 1 | 0 | Selects internal clock mode. |
| 0 | 1 | Reserved for future use. |
| 1 | 1 | No power-down between conversions, device always powered. Selects external clock mode. |

TABLE V. Power-Down Selection.

Clock Modes

The ADS8345 can be used with an external serial clock or an internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the device. Internal clock mode is selected when PD1 is HIGH and PD0 is LOW.

If the user decides to switch from one clock mode to the other, an extra conversion cycle will be required before the ADS8345 can switch to the new mode. The extra cycle is required because the PD0 and PD1 control bits need to be written to the ADS8345 prior to the change in clock modes.

When power is first applied to the ADS8345, the user must set the desired clock mode. It can be set by writing PD1 = 1 and PD0 = 0 for internal clock mode or PD1 = 1 and PD0 = 1 for external clock mode. After enabling the required clock mode, only then should the ADS8345 be set to power-down between conversions (i.e., PD1 = PD0 = 0). The ADS8345 maintains the clock mode it was in prior to entering the power-down modes.

External Clock Mode

In external clock mode, the external clock not only shifts data in and out of the ADS8345, it also controls the A/D conversion steps. BUSY will go HIGH for one clock period after the last bit of the control byte is shifted in. Successive-approximation bit decisions are made and appear at D_{OUT} on each of the next 16 DCLK falling edges (see Figure 6). Figure 7 shows the BUSY timing in external clock mode.

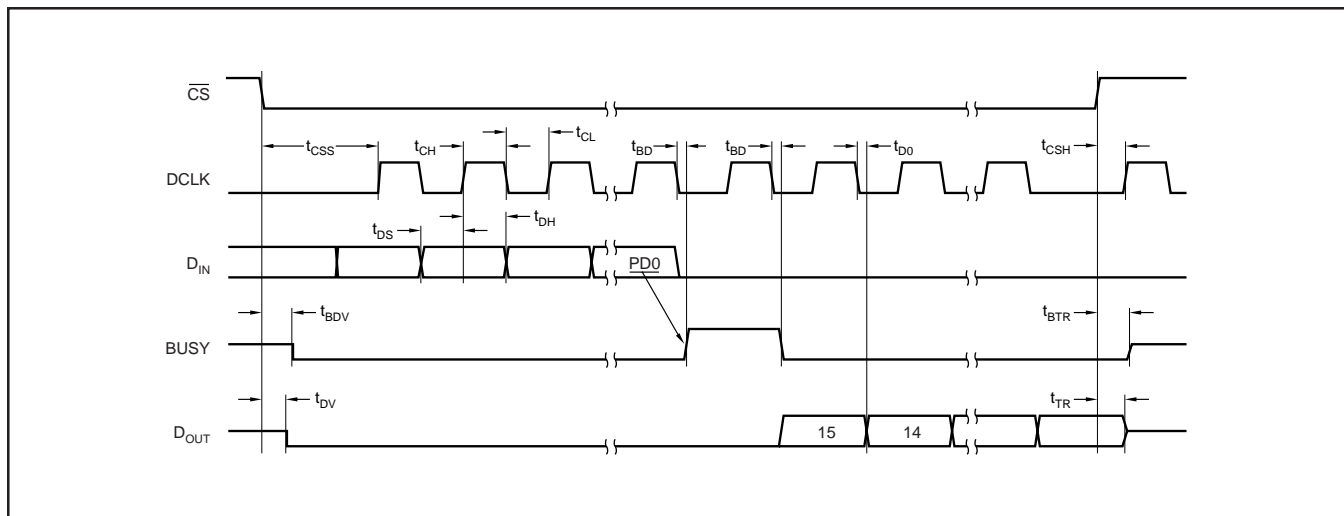


FIGURE 7. Detailed Timing Diagram.

Since one clock cycle of the serial clock is consumed with BUSY going HIGH (while the MSB decision is being made), 16 additional clocks must be given to clock out all 16 bits of data; thus, one conversion takes a minimum of 25 clock cycles to fully read the data. Since most microprocessors communicate in 8-bit transfers, this means that an additional transfer must be made to capture the LSB.

There are two ways of handling this requirement. One is where the beginning of the next control byte appears at the same time the LSB is being clocked out of the ADS8345 (see Figure 6). This method allows for maximum throughput and 24 clock cycles per conversion.

The other method is shown in Figure 8, which uses 32 clock cycles per conversion; the last seven clock cycles simply shift out zeros on the D_{OUT} line. BUSY and D_{OUT} go into a high-impedance state when \overline{CS} goes HIGH; after the next \overline{CS} falling edge, BUSY will go LOW.

Internal Clock Mode

In internal clock mode, the ADS8345 generates its own conversion clock internally. This relieves the microprocessor from having to generate the SAR conversion clock and allows the conversion result to be read back at the processor's convenience, at any clock rate from 0MHz to 2.0MHz. BUSY goes LOW at the start of a conversion and then returns HIGH when the conversion is complete. During the conversion, BUSY will remain LOW for a maximum of 8 μ s. Also, during the conversion, DCLK should remain LOW to achieve the best noise performance. The conversion result is stored in an internal register; the data may be clocked out of this register any time after the conversion is complete.

If \overline{CS} is LOW when BUSY goes LOW following a conversion, the next falling edge of the external serial clock will write out the MSB on the D_{OUT} line. The remaining bits (D14-D0) will be clocked out on each successive clock cycle following the MSB. If \overline{CS} is HIGH when BUSY goes LOW then the D_{OUT} line will remain in tri-state until \overline{CS} goes LOW, as shown in Figure 9. \overline{CS} does not need to remain LOW once a conversion has started. Note that BUSY is not tri-stated when \overline{CS} goes HIGH in internal clock mode.

Data can be shifted in and out of the ADS8345 at clock rates exceeding 2.4MHz, provided that the minimum acquisition time t_{ACQ} , is kept above 1.7 μ s.

Digital Timing

Figure 7 and Tables VI and VII provide detailed timing for the digital interface of the ADS8345.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|-----------|---|-----|-----|-----|---------|
| t_{ACQ} | Acquisition Time | 1.5 | | | μ s |
| t_{DS} | D _{IN} Valid Prior to DCLK Rising | 100 | | | ns |
| t_{DH} | D _{IN} Hold After DCLK HIGH | 10 | | | ns |
| t_{DO} | DCLK Falling to D _{OUT} Valid | | | 200 | ns |
| t_{DV} | \overline{CS} Falling to D _{OUT} Enabled | | | 200 | ns |
| t_{TR} | \overline{CS} Rising to D _{OUT} Disabled | | | 200 | ns |
| t_{CSS} | \overline{CS} Falling to First DCLK Rising | 100 | | | ns |
| t_{CSH} | \overline{CS} Rising to DCLK Ignored | 0 | | | ns |
| t_{CH} | DCLK HIGH | 200 | | | ns |
| t_{CL} | DCLK LOW | 200 | | | ns |
| t_{BD} | DCLK Falling to BUSY Rising | | | 200 | ns |
| t_{BDV} | \overline{CS} Falling to BUSY Enabled | | | 200 | ns |
| t_{BTR} | \overline{CS} Rising to BUSY Disabled | | | 200 | ns |

TABLE VI. Timing Specifications (+V_{CC} = +2.7V to 3.6V, T_A = -40°C to +85°C, C_{LOAD} = 50pF).

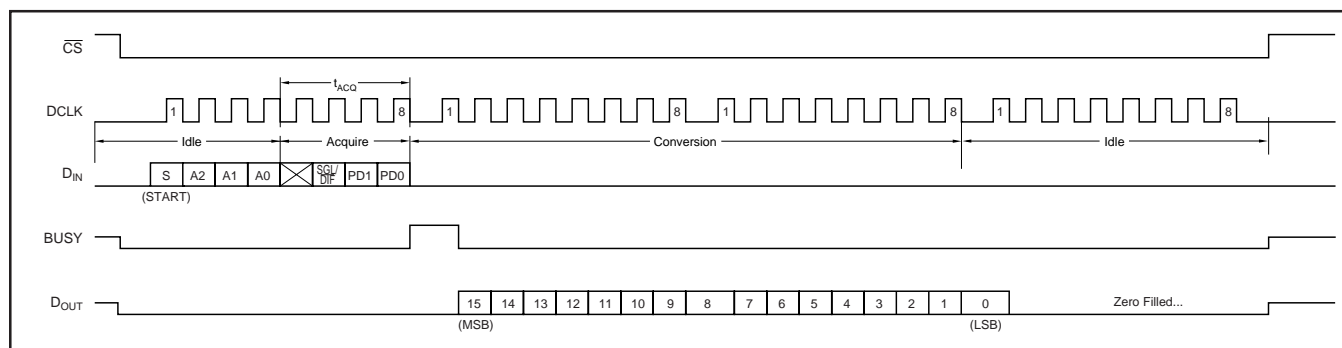


FIGURE 8. External Clock Mode, 32 Clocks Per Conversion.

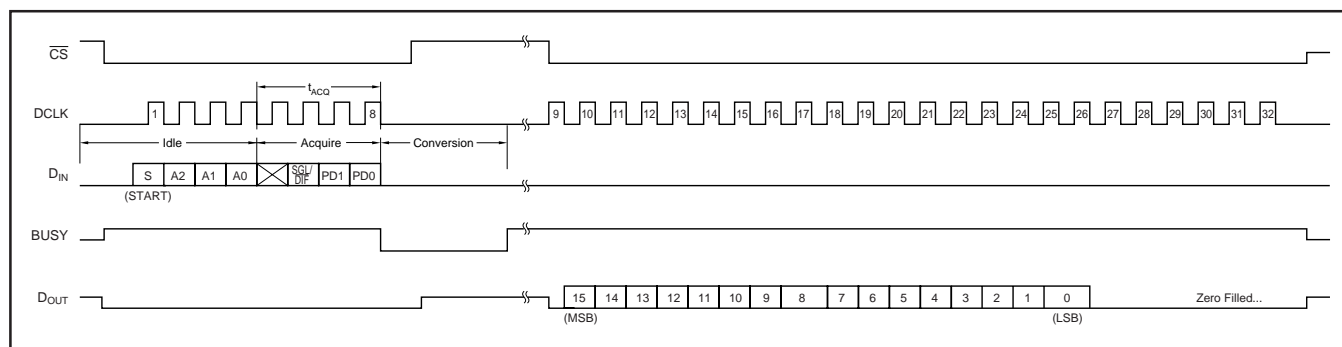


FIGURE 9. Internal Clock Mode Timing.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|-----------|--|-----|-----|-----|---------|
| t_{ACQ} | Acquisition Time | 1.7 | | | μ s |
| t_{DS} | D_{IN} Valid Prior to DCLK Rising | 50 | | | ns |
| t_{DH} | D_{IN} Hold After DCLK HIGH | 10 | | | ns |
| t_{DO} | DCLK Falling to D_{OUT} Valid | | | 100 | ns |
| t_{DV} | \overline{CS} Falling to D_{OUT} Enabled | | | 70 | ns |
| t_{TR} | \overline{CS} Rising to D_{OUT} Disabled | | | 70 | ns |
| t_{CSS} | \overline{CS} Falling to First DCLK Rising | 50 | | | ns |
| t_{CSH} | \overline{CS} Rising to DCLK Ignored | 0 | | | ns |
| t_{CH} | DCLK HIGH | 150 | | | ns |
| t_{CL} | DCLK LOW | 150 | | | ns |
| t_{BD} | DCLK Falling to BUSY Rising | | | 100 | ns |
| t_{BDV} | \overline{CS} Falling to BUSY Enabled | | | 70 | ns |
| t_{BTR} | \overline{CS} Rising to BUSY Disabled | | | 70 | ns |

TABLE VII. Timing Specifications (+ V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, and C_{LOAD} = 50pF).

Data Format

The output data from the ADS8345 is in Binary Two's Complement format, as shown in Table VIII. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT BINARY TWO'S COMPLEMENT | |
|-----------------------------|--------------------------|---|----------|
| Full-Scale Range | $2 \cdot V_{REF}$ | | |
| Least Significant Bit (LSB) | $2 \cdot V_{REF}/65536$ | | |
| | | BINARY CODE | HEX CODE |
| +Full-Scale | $+V_{REF} - 1\text{LSB}$ | 0111 1111 1111 1111 | 7FFF |
| Midscale | 0V | 0000 0000 0000 0000 | 0000 |
| Midscale - 1LSB | $0V - 1\text{LSB}$ | 1111 1111 1111 1111 | FFFF |
| -Full-Scale | $-V_{REF}$ | 1000 0000 0000 0000 | 8000 |

TABLE VIII. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

There are three power modes for the ADS8345: full-power (PD1-PD0 = 11B), auto power-down (PD1-PD0 = 00B), and shutdown (SHDN LOW). The effects of these modes varies depending on how the ADS8345 is being operated. For example, at full conversion rate and 24-clocks per conversion, there is very little difference between full-power mode and auto power-down; a shutdown will not lower power dissipation.

When operating at full-speed and 24-clocks per conversion (see Figure 6), the ADS8345 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversions are simply done less often, then the difference between the two modes is dramatic. In the latter case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and \overline{CS} is LOW while the ADS8345 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping \overline{CS} HIGH.

Operating the ADS8345 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. \overline{SHDN} can be used to force an immediate power-down.

NOISE

The noise floor of the ADS8345 itself is rather low (see Figures 10 and 11). The ADS8345 was tested at both 5V and 2.7V, and in both the internal and external clock modes. A low-level DC input was applied to the analog-input pins and the converter was put through 5000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8345. This is true for all 16-bit, SAR-type, A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The $\pm 1\sigma$, $\pm 2\sigma$, and $\pm 3\sigma$ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the $\pm 3\sigma$ distribution, or 99.7%, of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8345, with 5 output codes for the $\pm 3\sigma$ distribution, will yield a $< \pm 0.83\text{LSB}$ transition noise at 5V operation. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be $< 50\mu\text{V}$.

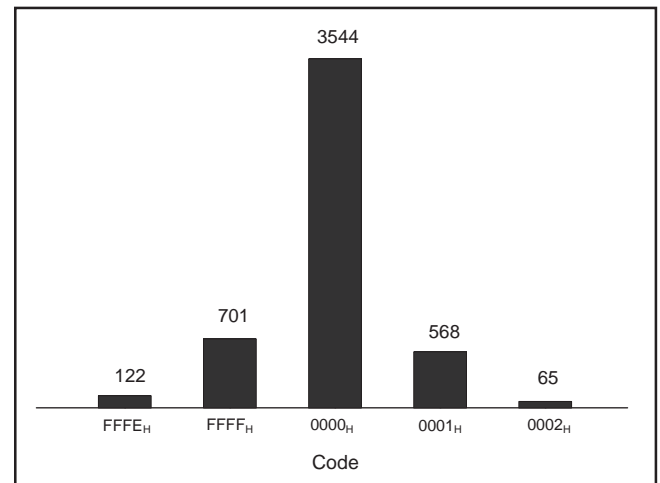


FIGURE 10. Histogram of 5000 Conversions of a DC Input at the Code Transition, 5V operation external clock mode. $V_{REF} = V_{COM} = 2.5V$.

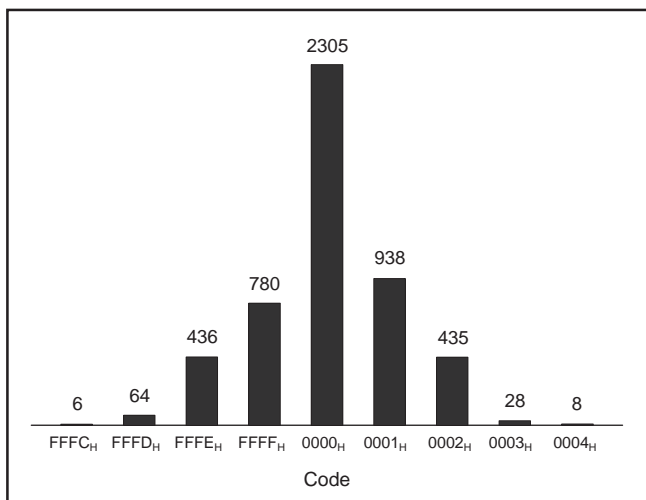


FIGURE 11. Histogram of 5000 Conversions of a DC Input at the Code Center, 2.7V operation external clock mode. $V_{REF} = V_{COM} = 1.25V$.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by $1/2$ to $\pm 0.25LSBs$. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio will improve 3dB.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8345 circuitry. This is particularly true if the reference voltage is LOW and/or the conversion rate is HIGH.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the

output of the analog comparator. Thus, during any single conversion for an n -bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS8345 should be clean and well bypassed. A $0.1\mu F$ ceramic bypass capacitor should be placed as close to the device as possible. In addition, a $1\mu F$ to $10\mu F$ capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a $0.1\mu F$ capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS8345 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

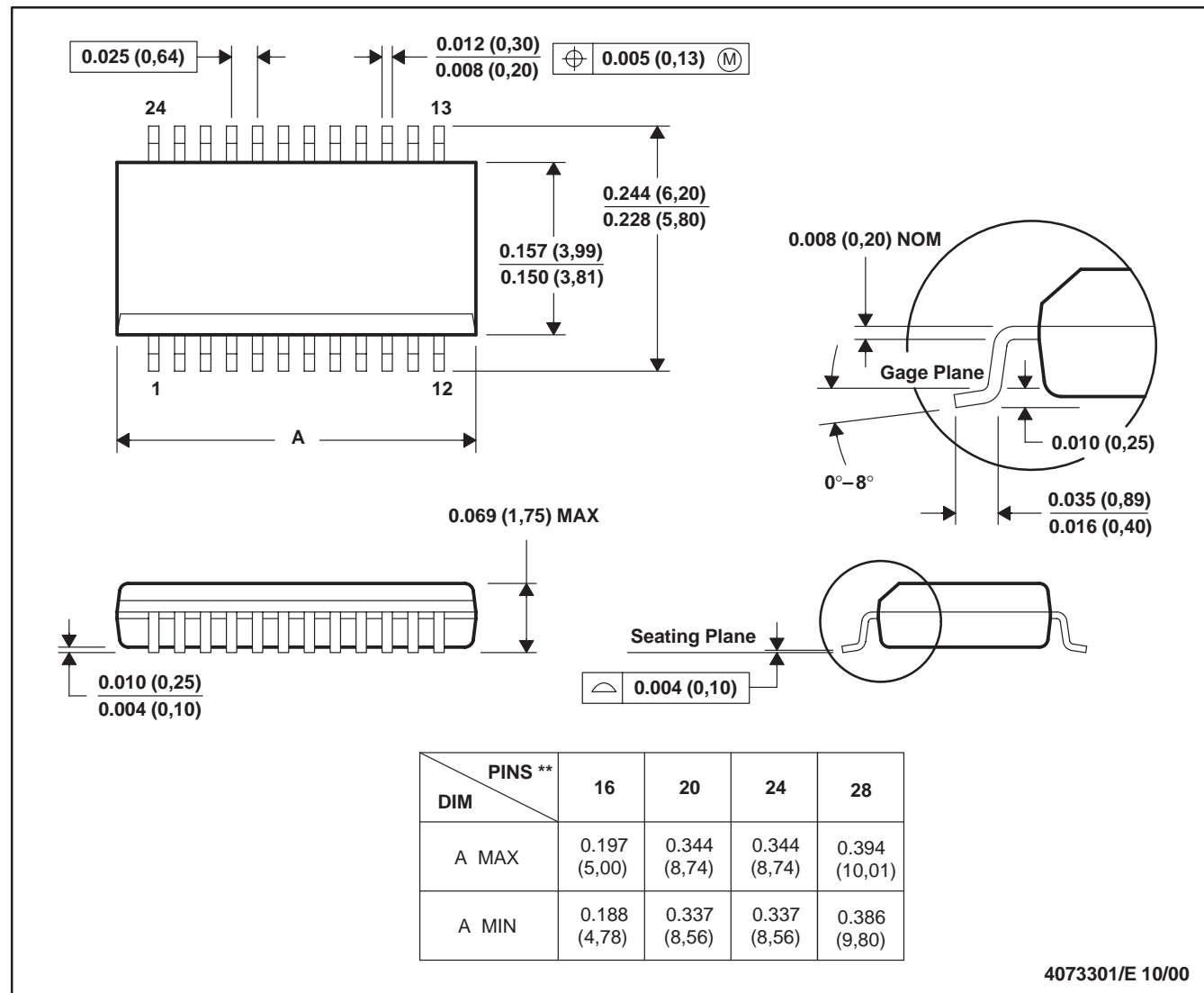
The ADS8345 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

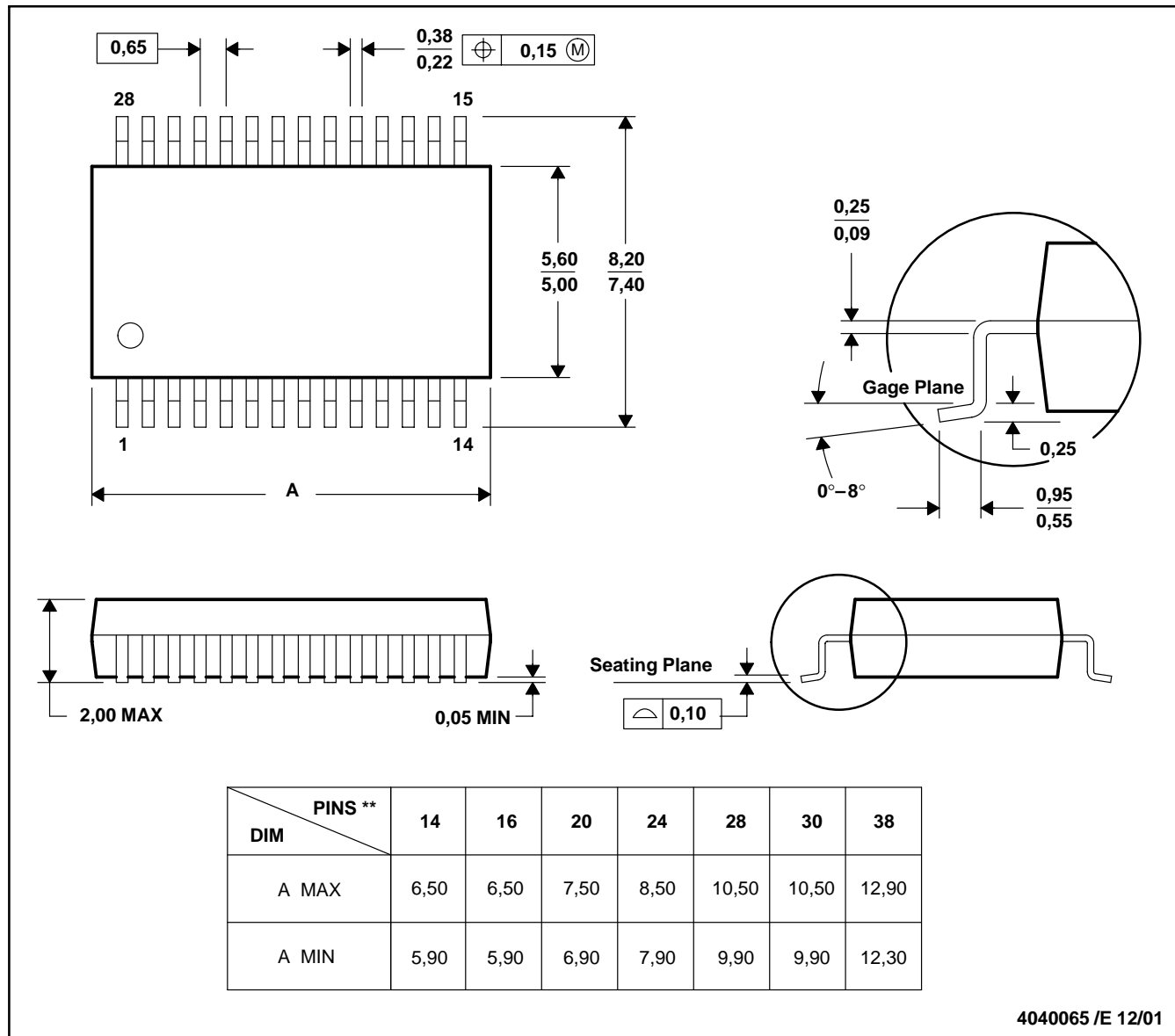


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|---------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| ADS8345E | ACTIVE | SSOP/ QSOP | DBQ | 20 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345E/2K5 | ACTIVE | SSOP/ QSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345E/2K5G4 | ACTIVE | SSOP/ QSOP | DBQ | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345EB | ACTIVE | SSOP/ QSOP | DBQ | 20 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345EBE4 | ACTIVE | SSOP/ QSOP | DBQ | 20 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345EE4 | ACTIVE | SSOP/ QSOP | DBQ | 20 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345N | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345N/1K | ACTIVE | SSOP | DB | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345N/1KG4 | ACTIVE | SSOP | DB | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345NB | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345NBG4 | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS8345NG4 | ACTIVE | SSOP | DB | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

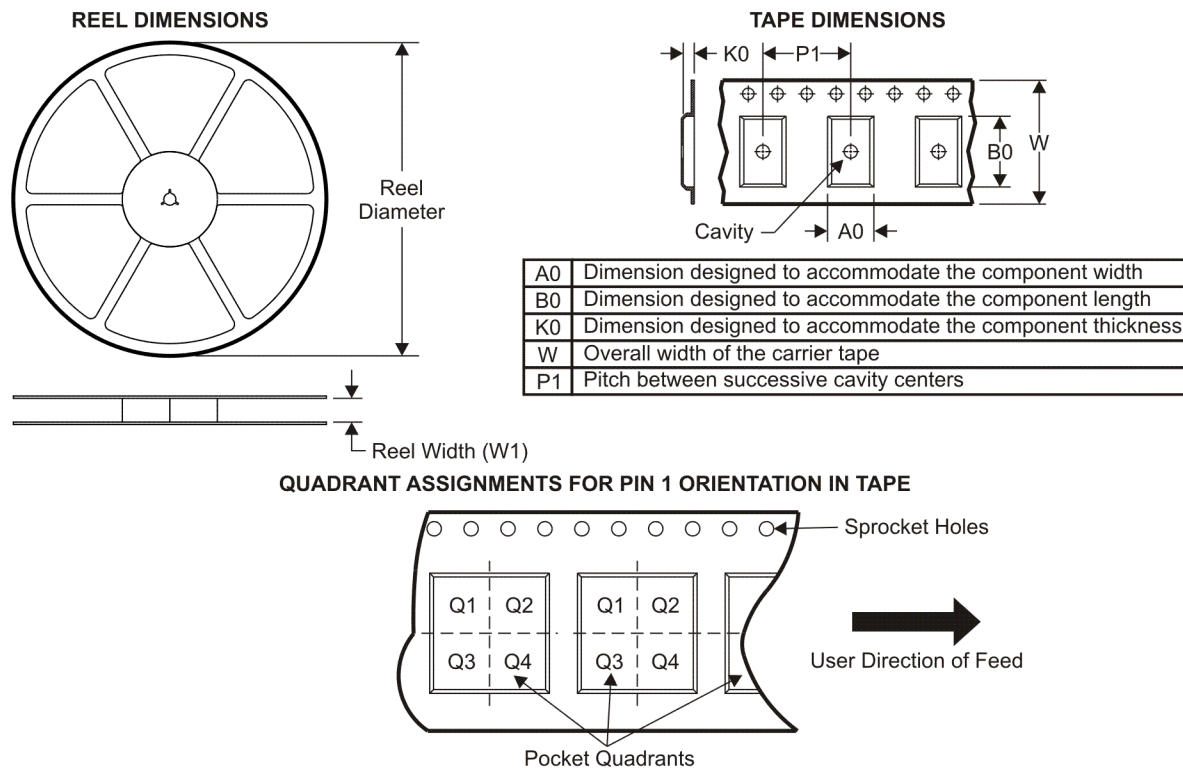
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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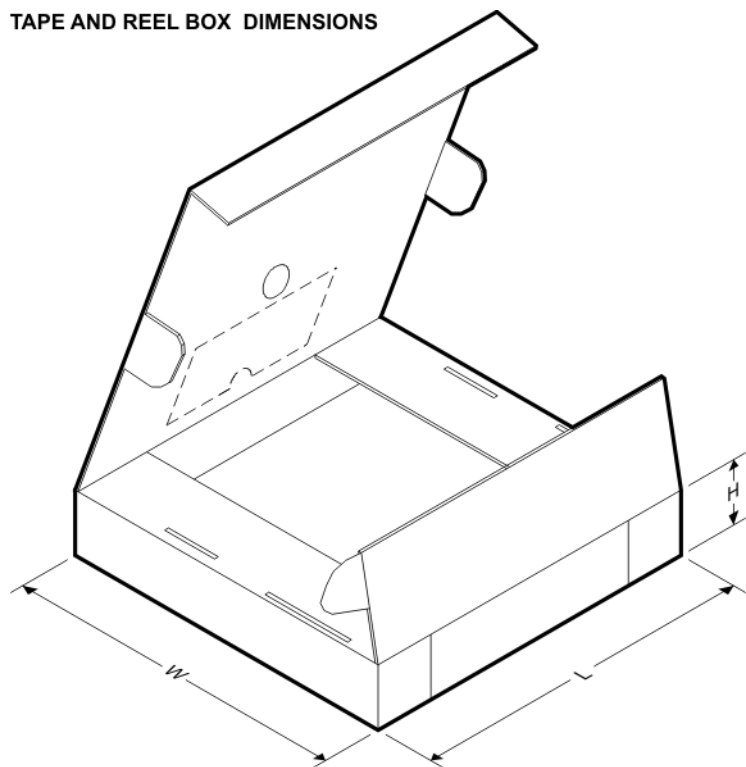
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS8345E/2K5 | SSOP/QSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| ADS8345N/1K | SSOP | DB | 20 | 1000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



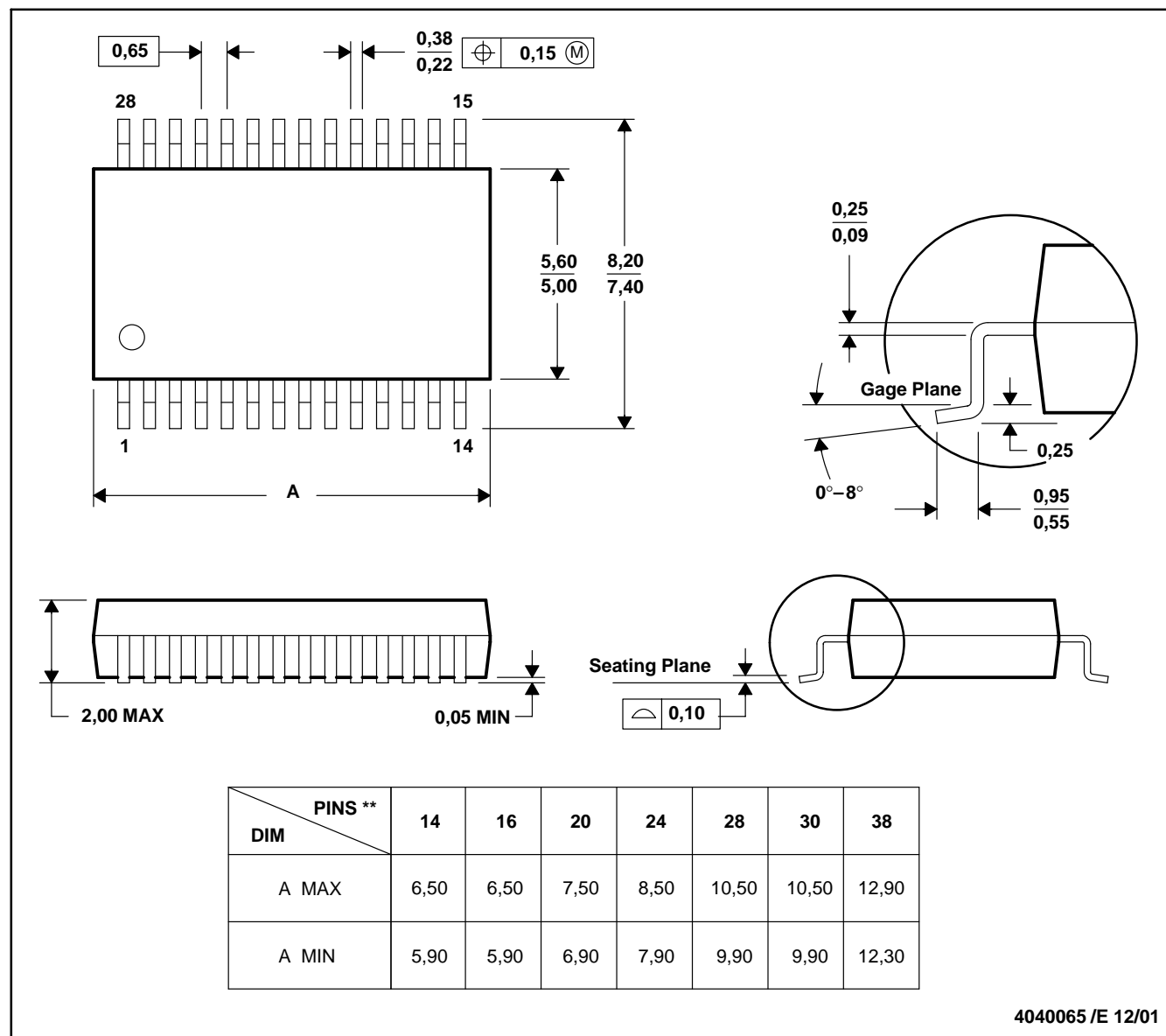
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS8345E/2K5 | SSOP/QSOP | DBQ | 20 | 2500 | 346.0 | 346.0 | 33.0 |
| ADS8345N/1K | SSOP | DB | 20 | 1000 | 346.0 | 346.0 | 33.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

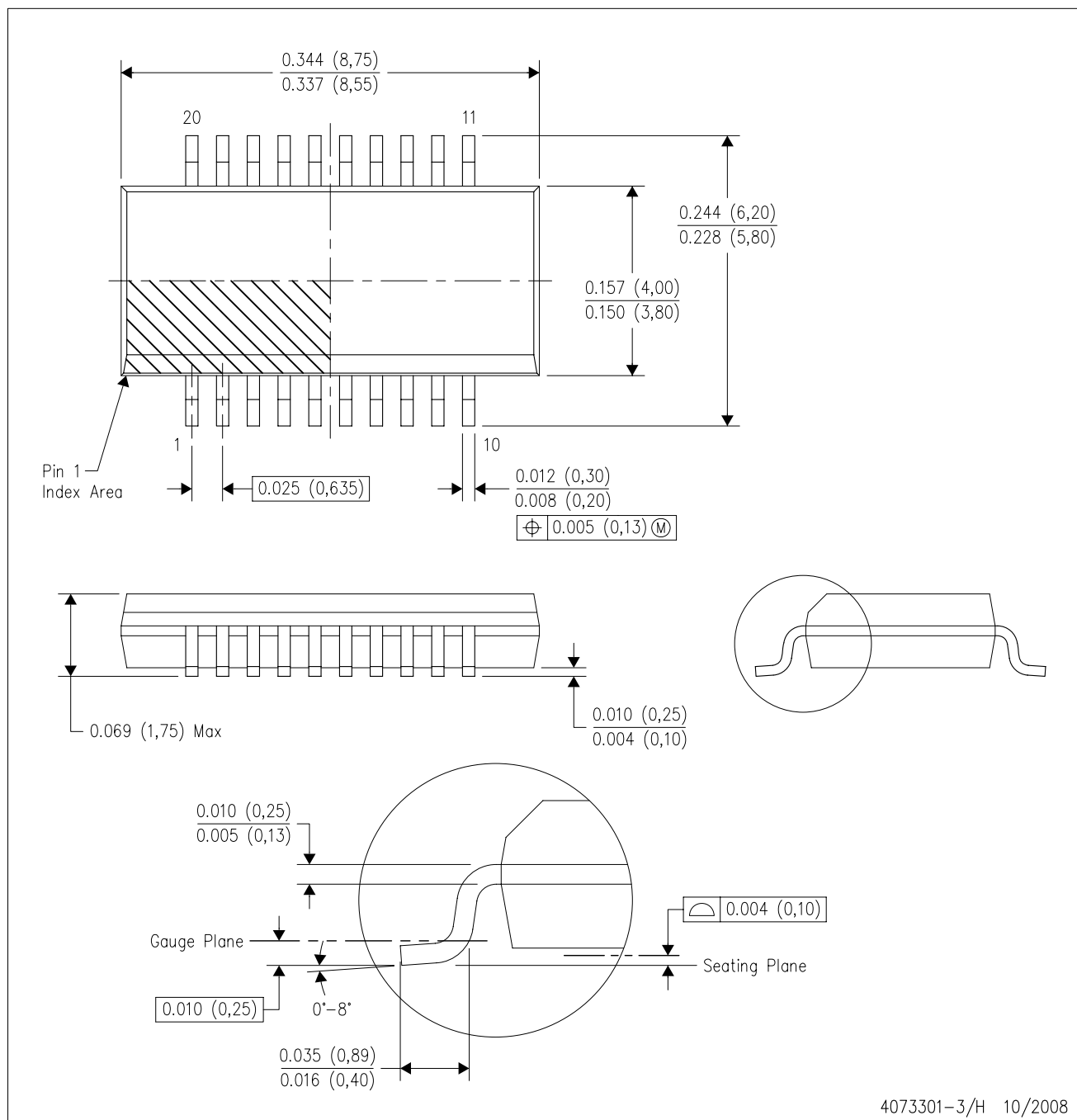
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

DBQ (R-PDSO-G20)

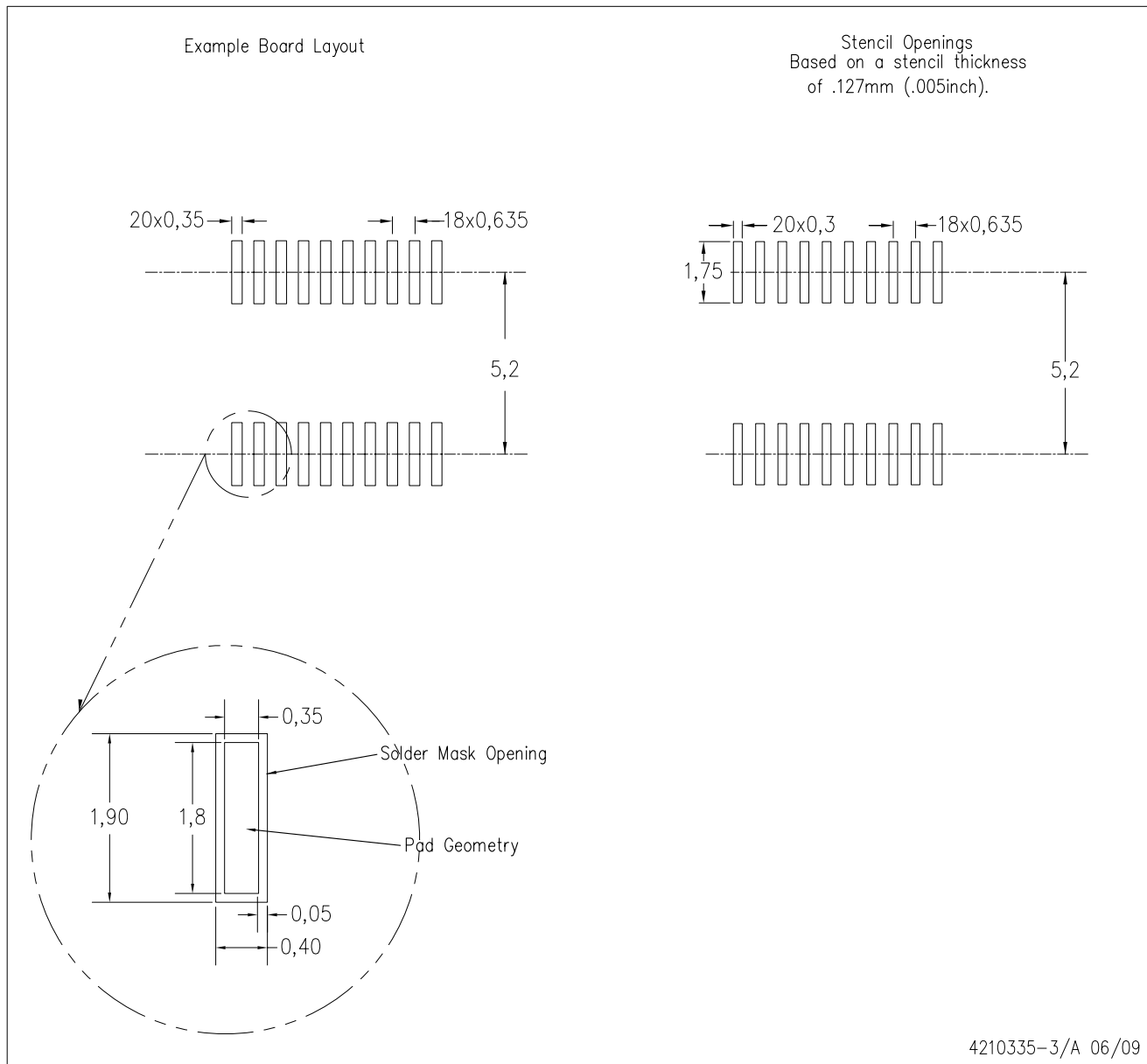
PLASTIC SMALL-OUTLINE PACKAGE



4073301-3/H 10/2008

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - Falls within JEDEC MO-137 variation AD.

DBQ (R-PDSO-G20)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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