GD7965 Specification

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GD7965

All-in-one driver IC with Timing Controller for White/Black/Red Dot-Matrix Micro-Cup EPD

INTRODUCTION

The GD7965 is an all-in-one driver with timing controller for EPD. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VDH/VDL (±2.4V~±15.0V) and VDHR (2.4V~15.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

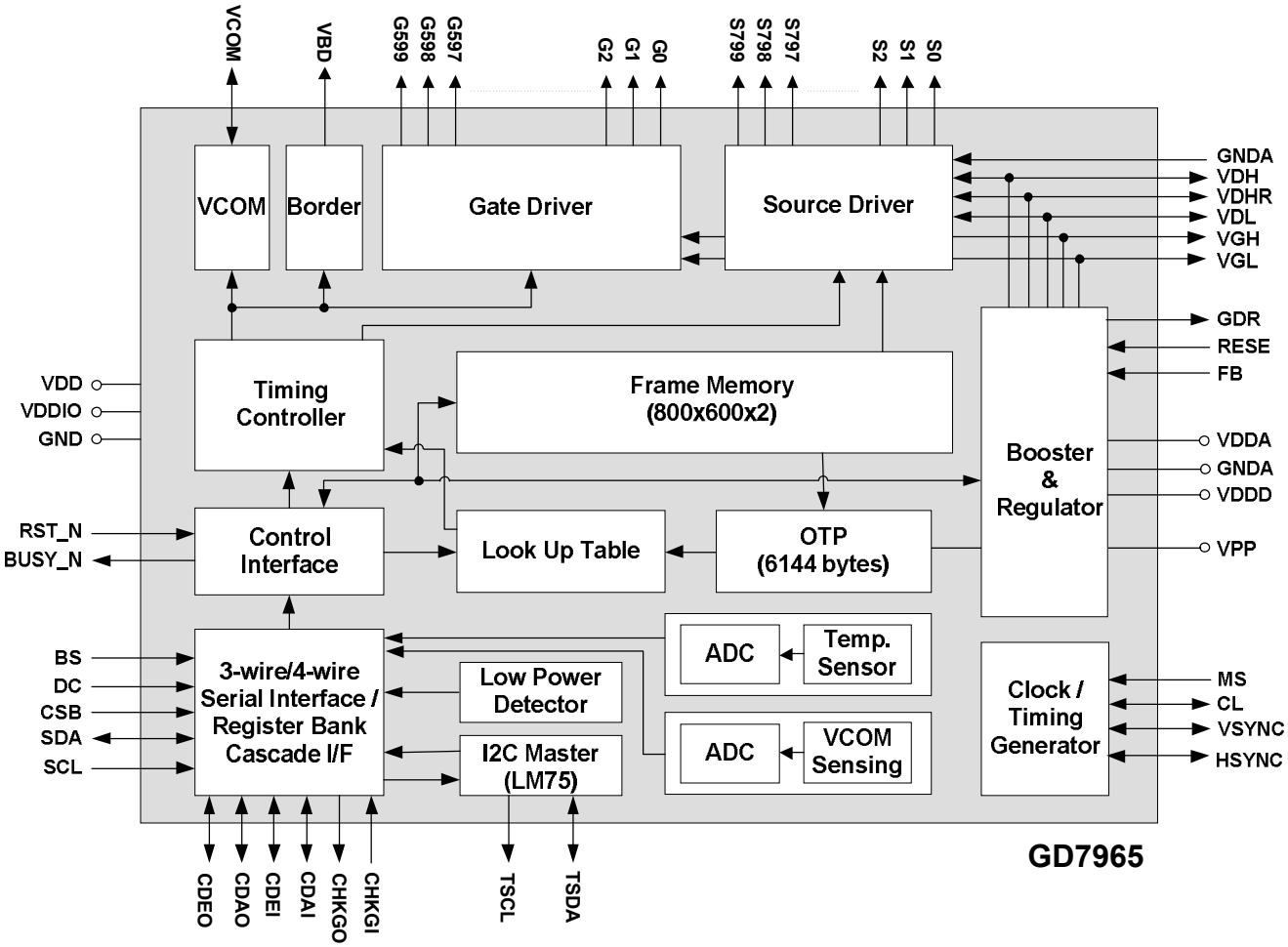
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for EPD
- Timing controller supports several resolutions
  - Up to 800 source x 600 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 800 x 600 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 °C ± 2.0°C / 8-bit status
  - Off-Chip: -55~125°C ± 2.0°C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection
  - V_{DD} < 2.5V or 2.4V or 2.3V or 2.2V (by setting)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (7-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +9V~+12V, +17V~+20V (programmable)
  - VGL: -9V~-12V, -17V~-20V (programmable)
  - VDH: +2.4 ~ +15.0V (programmable, black/white)
  - VDL: -2.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +15.0V (programmable, red)
- Supply voltage: 2.3~ 3.6V
- OTP: 6K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 14 μM ± 2 μM
  - Bump space: 1 μM ± 3 μM
  - Bump surface: 1200 μM^2

Remark: The inspection standard of the product appearance is based on WF's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
GD7965cGAA-U0X3-3	IC thickness: 300uM, with 3” double-faced tray
GD7965cGAA-U0X3-4	IC thickness: 300uM, with 4” double-faced tray

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, Waveshare has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. Waveshare assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	10	PWR	Digital power
VDDA	13	PWR	Analog power
VDDIO	18	PWR	IO power
VDDDO	8	PWR	Digital power output (1.8V)
VDDD (VDDDI)	8	PWR	Digital power input (1.8V)
VPP	10	PWR	OTP program power (7.75V)
VDM	8	PWR	Analog Ground.
GND	19	PWR	Digital Ground.
GNDA	15	PWR	Analog Ground
LDO PINS			
VDH	12	I/O	Positive source driver Voltage (+2.4V ~ +15V)
VDHR	16	I/O	Positive source driver voltage for Red (+2.4V ~ +15V)
VDL	12	I/O	Negative source driver voltage (-2.4V ~ -15V)
CONTROL INTERFACE PINS			
BS	2	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. H: 3-wire interface.
RST_N	2	I (Pull-up)	Global reset pin. Low: active. When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 50us.
MS	2	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	2	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDEI	2	I/O	Cascade signal pin. Leave it open if not used.
CDEO	2	I/O	Cascade signal pin. Leave it open if not used.
CDAI	2	I/O	Cascade data pin. Leave it open if not used.
CDAO	2	I/O	Cascade data pin. Leave it open if not used.
MM	2	I	Cascade setting pin. Leave it open if not used.
LSYNC	2	I/O	Cascade sync pin. Leave it open if not used.
M1M2_SYNC	2	I/O	Cascade sync pin. Leave it open if not used.
M2M1_SYNC	2	I/O	Cascade sync pin. Leave it open if not used.
BUSY_N	2	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.

Pin (Pad) Name	Pin Count	Type	Description
MCU INTERFACE (SPI) PINS			
CSB	2	I	Serial communication chip select.
SDA	2	I/O	Serial communication data input/output
SDA1	2	I	Serial communication data input for dual mode. Leave open if single SPI mode is used.
SCL	2	I	Serial communication clock input.
DC	2	I	Command/Data input. L: command H: data Connect to GND if BS=High.
I^2C INTERFACE			
TSCL	2	O (open-drain)	I^2C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I^2C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S799 (S<0>~S<799>)	800	O	Source driver output signals.
G0~G599 (G<0>~G<599>)	600	O	Gate driver output signals.
VCOM	32	O	VCOM output.
VBD (VBD<0>, VBD<1>)	1, 1	O	Border output pins.
BOOSTER PINS			
GDR	14	O	N-MOS gate control
RESE	4	I	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	14	I/O	Positive Gate voltage.
VGL	14	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	2	I (Pull-down)	Check panel break input. Leave open if it is not used.
CHKGO	2	O	Check panel break output. Leave open if it is not used.
RESERVED PINS			
VSYNC	2	O	Reserved pins. Leave it floating.
HSYNC	2	O	Reserved pins. Leave it floating.
TEST1~TEST3	2x3	I	Reserved pins. Leave it floating
TEST4~TEST7	2x4	O	Reserved pins. Leave it floating.
TEST8~TEST13	2x6	I	Reserved pins. Leave it floating.
DUMMY	108	-	Reserved pins. Leave it floating.
GD<0>~GD<3>	1x4		Reserved pins. Leave it floating.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	--	--	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	#	#	#	BD_EN, VSR_EN, VS_EN, VG_EN	07H
		0	1	#	--	--	#	--	#	#	#	VPP_EN, VCOM_SLEW, VG_LVL[2:0]	17H
		0	1	--	--	#	#	#	#	#	#	VDH_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDL_LVL[5:0]	3AH
		0	1	--	--	#	#	#	#	#	#	VDHR_LVL[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC1[5:0]	17H
		0	1	#	--	#	#	#	#	#	#	PHC2_EN, BT_PHC2[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (800x600):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (800x600):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Dual SPI	0	0	0	0	0	1	0	1	0	1		15H
		1	1	--	--	#	#	--	--	--	--	MM_EN, DUSPI_EN	00H
14	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
15	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
16	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2BH
		0	1	--	--	--	--	--	--	#	#	ATRED, NORED	00H
		0	1	#	#	--	--	--	--	--	--	KWE[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	KWE[7:0]	00H
17	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	06H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
18	Temperature Sensor Calibration (TSC)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**		**40H**
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
19	Temperature Sensor Selection (TSE)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**		**41H**
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
20	Temperature Sensor Write (TSW)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**		**42H**
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
21	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43H**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
22	Panel Break Check (PBC)	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**		**44H**
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
23	VCOM and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50H**
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31H
		0	1	--	--	--	--	#	#	#	#	CDI[3:0]	07H
24	Lower Power Detection (LPD)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**		**51H**
		1	1	--	--	--	--	--	--	--	#	LPD	01H
25	End Voltage Setting (EVS)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**		**52H**
		0	1	--	--	--	--	#	--	#	#	VCEND, BDEND[1:0]	02H
26	TCON setting (TCON)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**60H**
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
27	Resolution setting (TRES)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**		**61H**
		0	1	--	--	--	--	--	--	#	#	HRES[9:8]	03H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	20H
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02H
		0	1	#	#	#	#	#	#	#	#		58H
28	Gate/Source Start setting (GSST)	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**65H**
		0	1	--	--	--	--	--	--	#	#	HST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	VST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
29	Revision (REV)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**		**70H**
		1	1	#	#	#	#	#	#	#	#	PROD_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	PROD_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:16]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	0CH
30	Get Status (FLG)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**		**71H**
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I^{2}C_ERR, I^{2}C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
31	Auto Measurement VCOM (AMV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**		**80H**
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
32	Read VCOM Value (VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81H**
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
33	VCOM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82H**
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
34	Partial Window (PTL)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**		**90H**
		0	1	--	--	--	--	--	--	#	#	HRST[9:8]	00H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	--	--	--	--	--	--	#	#	HRED[9:8]	03H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	1FH
		0	1	--	--	--	--	--	--	#	#	VRST[9:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	#	#	VRED[8:0]	02H
		0	1	#	#	#	#	#	#	#	#		57H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
35	Partial In (PTIN)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**1**		**91H**
36	Partial Out (PTOUT)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**		**92H**
37	Program Mode (PGM)	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**		**A0H**
38	Active Programming (APG)	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**		**A1H**
39	Read OTP (ROTP)	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**		**A2H**
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
40	Cascade Setting (CCSET)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**E0H**
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
41	Power Saving (PWS)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**		**E3H**
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
42	LVD Voltage Select (LVSEL)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**		**E4H**
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
43	Force Temperature (TSSET)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**E5H**
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H
44	Temperature Boundary Phase-C2 (TSBDRY)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**		**E7H**
		0	1	#	#	#	#	#	#	#	#	TSBDRY_PHC2[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by Wavesare, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	**-**	**-**	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	BD_EN	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	VPP_EN	-	-	VCOM _SLEW	-	VG_LVL[2:0]			17H
	0	1	-	-	VDH_LVL[5:0]						3AH
	0	1	-	-	VDL_LVL[5:0]						3AH
	0	1	-	-	VDHR_LVL[5:0]						03H

BD_EN: Border LDO enable
0 : Border LDO disable (Default)
Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR
1 : Border LDO enable
Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b:VBL(VCOM-VDH) 11b: VDHR

VSR_EN: Source LV power selection
0 : External source power from VDHR pins
1 : Internal DC/DC function for generating VDHR. (Default)

VS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VPP_EN: OTP program power selection
0 : External OTP program power from VPP pin
1 : OTP program power from internal power circuit.
Internal OTP program power voltage is selected by VDHR_LVL[5:0].

VCOM_SLEW: VCOM slew rate selection for voltage transition
0 : Slow slew rate
1 : Fast slew rate

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 **(Default)**	VGH=20V, VGL= -20V

VDH_LVL[5:0]: Internal VDH power selection for K/W pixel.(**Default value: 111010b**)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	**111010**	**14.0 V**
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL_LVL[5:0]: Internal VDL power selection for K/W pixel. (**Default value: 111010b**)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	**111010**	**-14.0 V**
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

VDHR_LVL[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 000011b**)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	**3.0 V**	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Internal Bandgap Set	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Booster Software Start Set	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]			17H
	0	1	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]			17H
	0	1	-	-	BT_PHC1[5:3]			BT_PHC1[2:0]			17H
	0	1	PHC2EN	-	BT_PHC2[5:3]			BT_PHC2[2:0]			17H

BT_PHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHB[5:3]: Driving strength of phase B

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BT_PHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

BT_PHC1[5:3]: Driving strength of phase C1

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BT_PHC1[2:0]: Minimum OFF time setting of GDR in phase C1

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

PHC2EN: Booster phase-C2 enable

0: Booster phase-C2 disable
Phase-C1 setting always is applied for booster phase-C.

1: Booster phase-C2 enable
If temperature > temperature boundary phase-C2(RE7h[7:0]), phase-C1 setting is applied for booster phase-C.
If temperature <= temperature boundary phase-C2(RE7h[7:0]), phase-C2 setting is applied for booster phase-C.

BT_PHC2[5:3]: Driving strength of phase C2

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BT_PHC2[2:0]: Minimum OFF time setting of GDR in phase C2

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	07H
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “K/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

(13) DUAL SPI MODE (DUSPI) (R15H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	1	0	1	15H
	0	1	-	-	MM_EN	DUSPI_EN	-	-	-	-	00H

This command sets dual SPI mode.

MM_EN: MM input pin definition enable.

0: MM input pin definition disable
1: MM input pin definition enable.

DUSPI_EN: Dual SPI mode enable.

0: Dual SPI mode disable (single SPI mode)
1: Dual SPI mode enable

(14) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(15) LUT OPTION (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	0	0	1	0	1	0	1	0	2AH
	0	1	STATE_XON[9:8]		-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H

This command sets XON control enable.

STATE_XON[9:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000 0000b: no All-Gate-ON

00 0000 0001b: State-1 All-Gate-ON

00 0000 0011b: State-1 and State2 All-Gate-ON

: :

(16) KW LUT OPTION (KWOPT) (R2BH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
KW LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	2BH
	0	1	-	-	-	-	-	-	ATRED	NORED	00H
	0	1	KWE[9:8]		-	-	-	-	-	-	00H
	0	1	KWE[7:0]								00H

This command sets KW LUT mechanism option in KWR mode's LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2, … .

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

00 0000 0001b: KW LUT enable in State-1

00 0000 0011b: KW LUT enable in State-1 and State2

00 0000 1011b: KW LUT enable in State-1, State2 and State-4

(17) PLL CONTROL (PLL) (R30H)

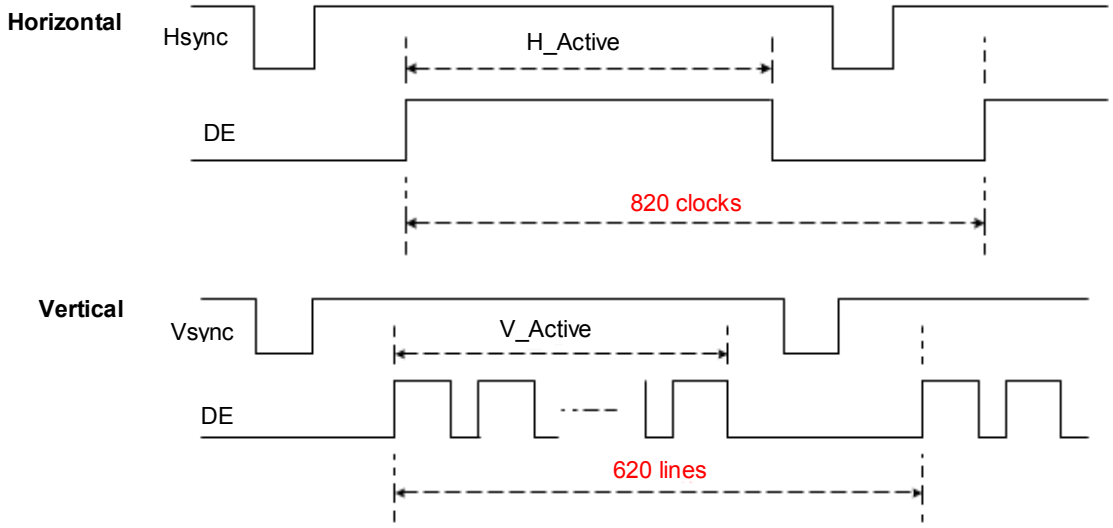
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	0	1	-	-	-	-	FRS[3:0]				06H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]: Frame rate setting

FRS	Frame rate
0000	5Hz
0001	10Hz
0010	15Hz
0011	20Hz
0100	30Hz
0101	40Hz
0110	**50Hz**
0111	60Hz

FRS	Frame rate
1000	70Hz
1001	80Hz
1010	90Hz
1011	100Hz
1100	110Hz
1101	130Hz
1110	150Hz
1111	200Hz



(18) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temp. (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temp. (°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(19) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calibration
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calibration
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(20) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(21) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(22) PANEL GLASS CHECK (PBC)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	44H
	1	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(23) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]		31h
	0	1	-	-	-	-	CDI[3:0]				07H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

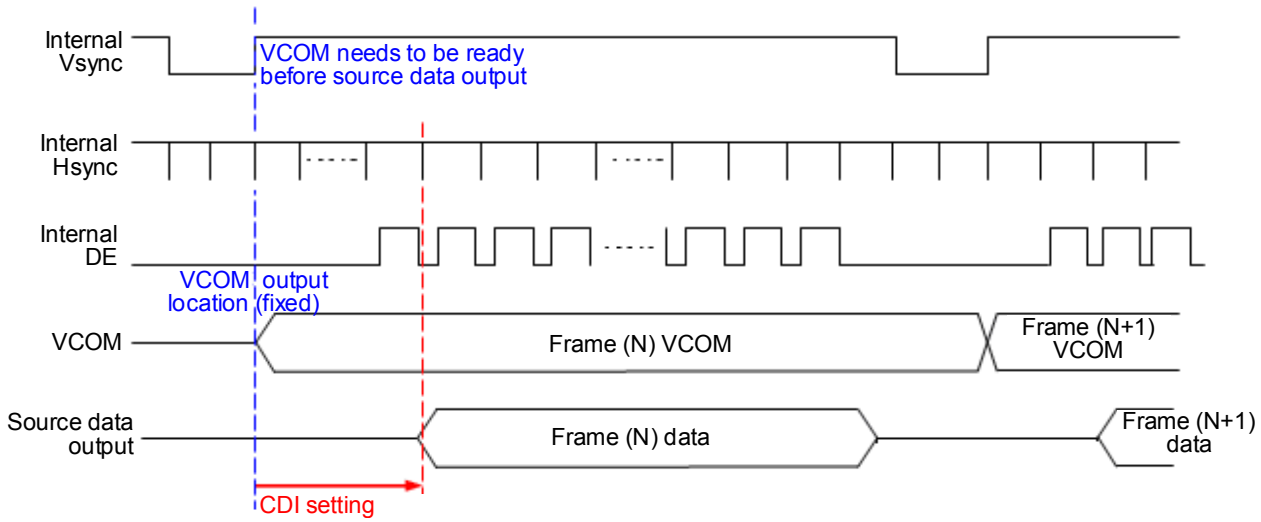
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



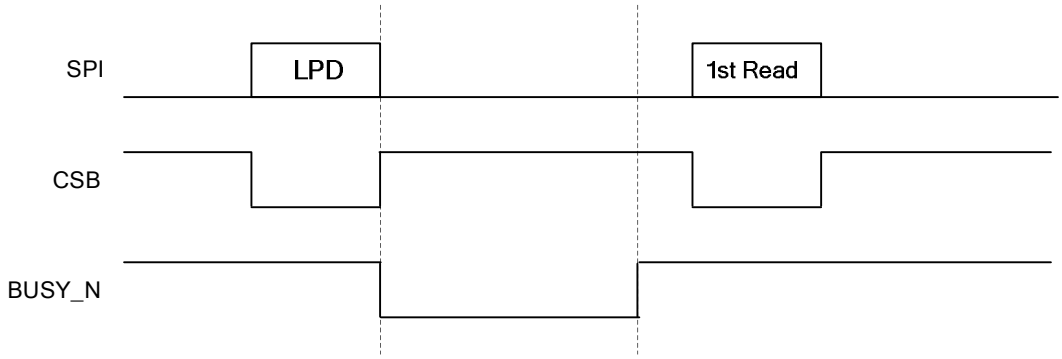
(24) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD} < 2.5V, 2.4V, 2.3V, or 2.2V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(25) END VOLTAGE SETTING (EVS) (R52H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
End Voltage Setting	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	52h
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]		02h

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM_DC 1b: floating

BDEND[1:0]: Border end voltage selection

00b: 0V 01b: 0V **10b: VCOM_DC** 11b: floating

(26) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

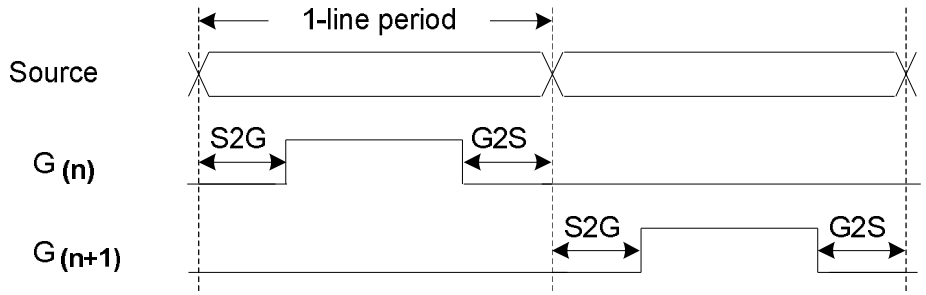
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 667 nS.



(27) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	-	-	-	-	-	-	HRES[9:8]		03h
	0	1	HRES[7:3]					**0**	**0**	**0**	20h
	0	1	-	-	-	-	-	-	VRES[9:8]		02h
	0	1	VRES[7:0]								58h

This command defines resolution setting.

HRES[9:3]: Horizontal Display Resolution (Value range: 01h ~ 64h)

VRES[9:0]: Vertical Display Resolution (Value range: 001h ~ 258h)

Active channel calculation, assuming HST[9:0]=0, VST[9:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[9:0] – 1

Source: First active source = S0;
Last active source = HRES[9:3]*8 – 1

Example: 128 (source) x 272 (gate), assuming HST[9:0]=0, VST[9:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[9:0] = 272, 272 – 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[9:3]=16, 16*8 – 1 = 127)

(28) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	-	-	-	-	-	-	HST[9:8]		00h
	0	1	HST[7:3]					**0**	**0**	**0**	00h
	0	1	-	-	-	-	-	-	VST[9:8]		00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[9:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 63h)

VST[9:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 257h)

Example : For 128(Source) x 240(Gate)
HST[9:3] = 4 (HST[9:0] = 4*8 = 32),
VST[9:0] = 32

Gate: First active gate = G32 (VST[9:0] = 32),
Last active gate = G271 (VRES[9:0] = 240, VST[9:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[9:0]= 32),
Last active source = S239 (HRES[9:0] = 128, HST[9:0] = 32, 128-1+32=239)

(29) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	PROD_REV[23:16]								FFh
	1	1	PROD_REV[15:8]								FFh
	1	1	PROD_REV[7:0]								FFh
	1	1	LUT_REV[23:16]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[7:0]								FFh
	1	1	CHIP_REV[7:0]								0Ch

The command reads the product revision, LUT revision and chip revision.

PROD_REV[23:0]: Product Revision. PROD_REV[23:0] is read from OTP address 0x0BDD ~ 0X0BDF or 0x17DD ~ 0x17DF.

LUT_REV[23:0]: LUT Revision. LUT_REV[23:0] is read from OTP address 0x0BE0 ~ 0X0BE2 or 0x17E0.~ 0x17E2.

CHIP_REV[7:0]: Chip Revision, fixed at 00001100b.

(30) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ Flag	I^2C_ERR	I^2C_ BUSYN	Data_ Flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_Flag: Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

Data_Flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(31) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command triggers auto VCOM sensing mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(32) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(33) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

(34) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	1	0	0	0	0	90h
	0	1	-	-	-	-	-	-	HRST[9:8]		00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	HRED[9:8]		03h
	0	1	HRED[7:3]					1	1	1	1Fh
	0	1	-	-	-	-	-	-	VRST[9:8]		00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	VRED[9:8]		02h
	0	1	VRED[7:0]								57h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[9:3]: Horizontal start channel bank. (Value range: 00h~63h)

HRED[9:3]: Horizontal end channel bank. (Value range: 00h~63h). HRED must be greater than HRST.

VRST[9:0]: Vertical start line. (Value range: 000h~257h)

VRED[9:0]: Vertical end line. (Value range: 000h~257h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(35) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(36) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(37) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(38) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

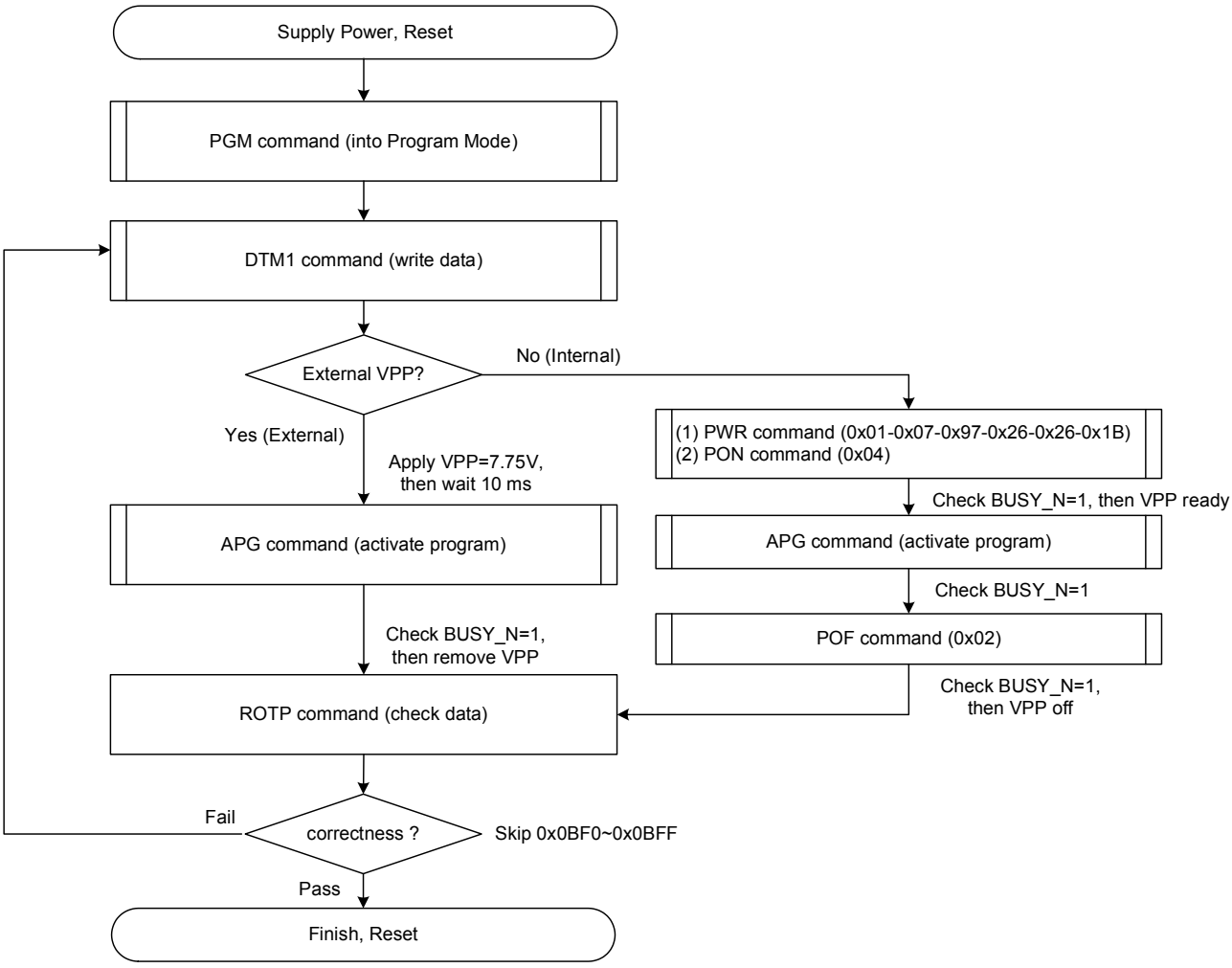
The BUSY_N flag would fall to 0 until the programming is completed.

(39) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.

(40) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

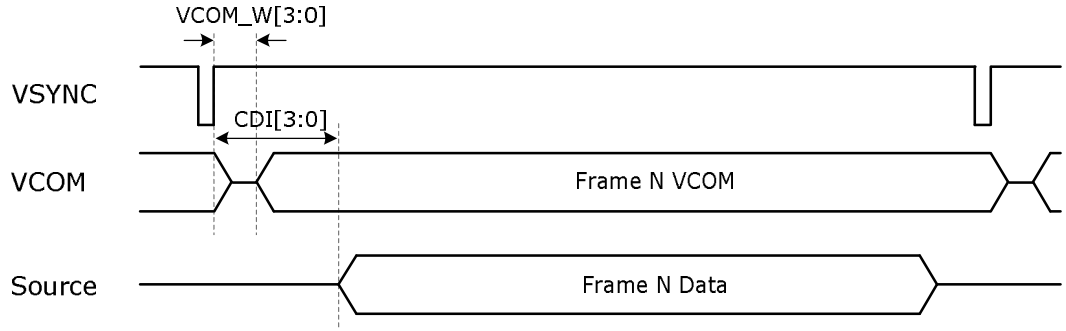
1: Output clock at CL pin to slave chip.

(41) POWER SAVING (PWS) (RE3H)

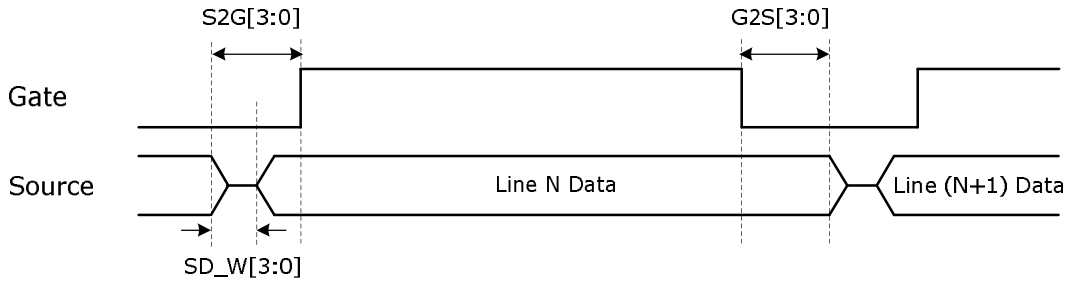
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (Unit: line period)



SD_W[3:0]: Source power saving width (Unit: 660nS)



(42) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(43) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

(44) TEMPERATURE BOUNDARY PHASE-C2 (TSBDRY) (RE7H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Boundary Phase-C2	0	0	1	1	1	0	0	1	1	1	E7h
	0	1	TSBDRY_PHC2[7:0]								00h

This command is used to set the temperature boundary to judge whether booster phase-C2 is applied or not.

HOST INTERFACES

WF8104 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

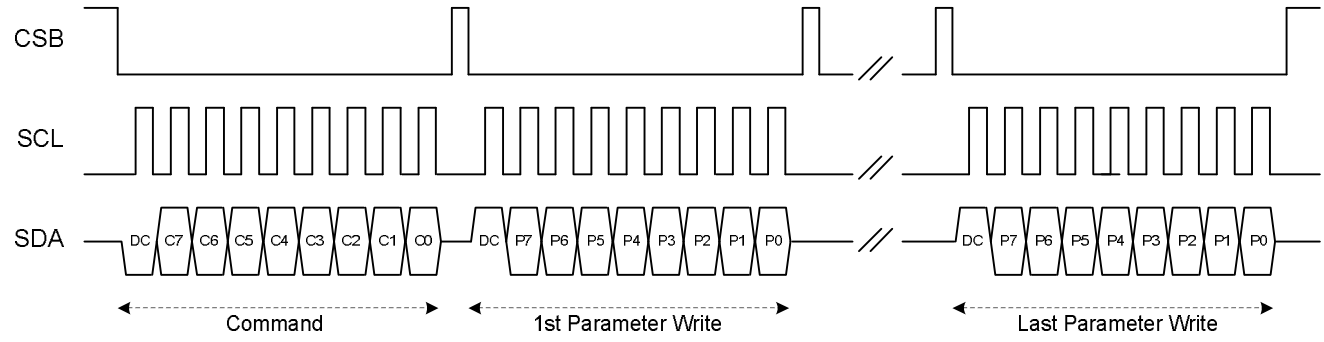


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

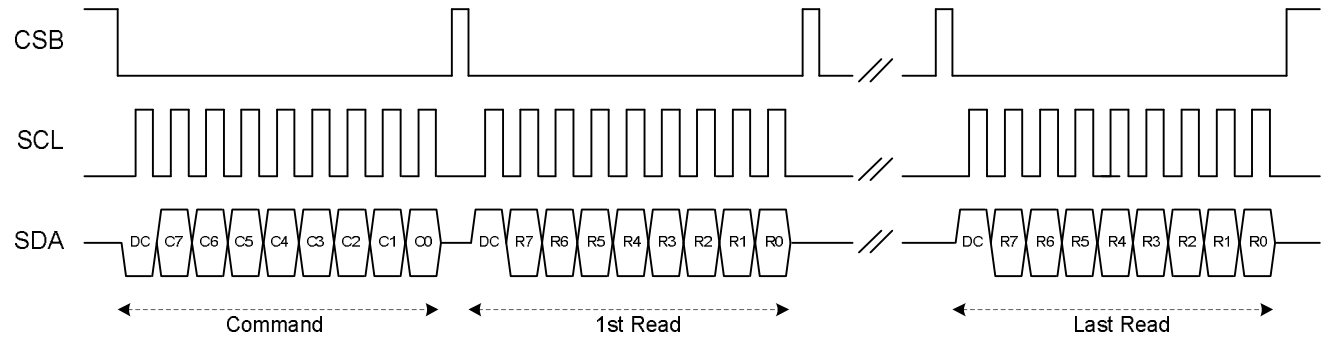


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

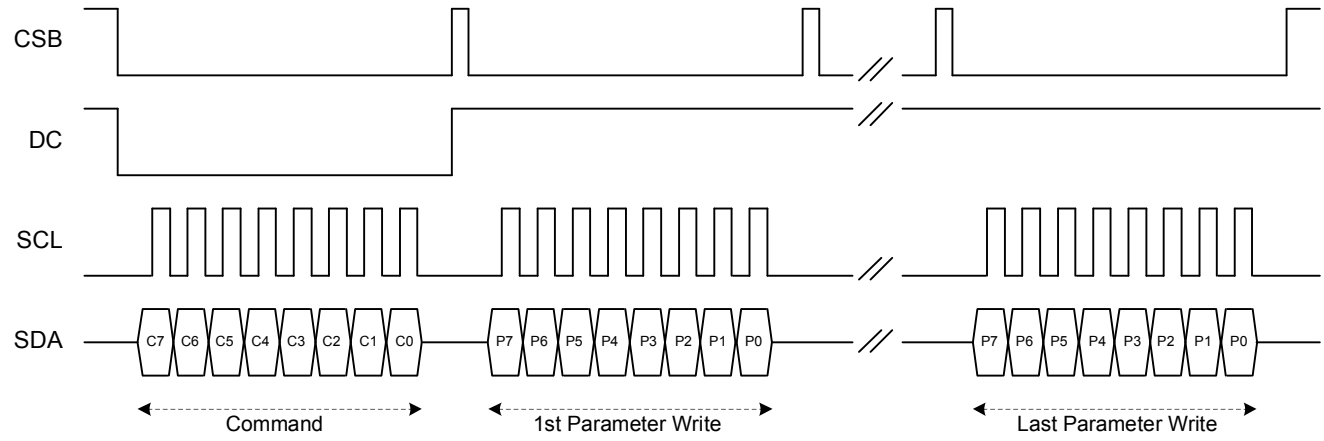


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

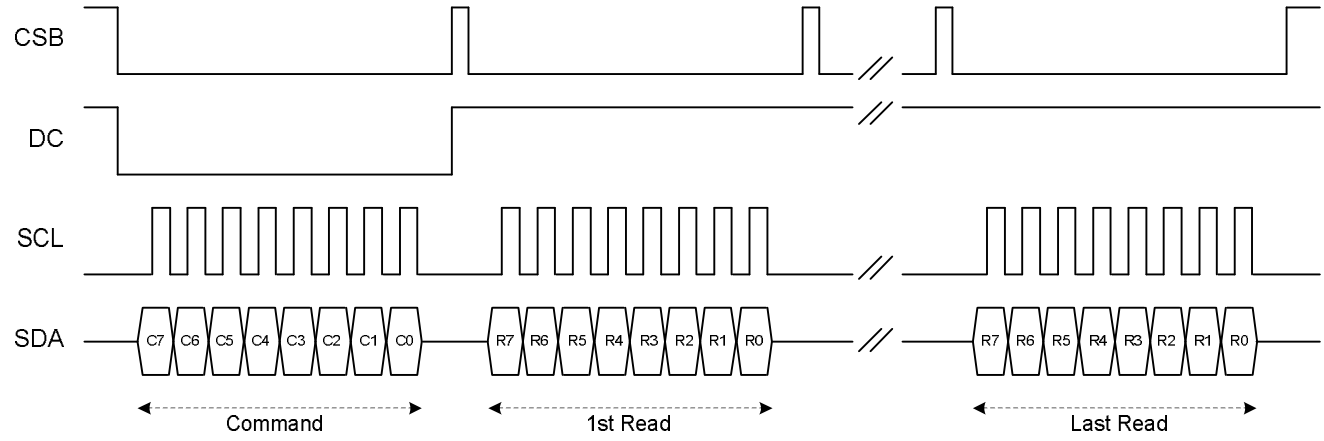


Figure: 4-wire SPI read operation

3 wire dual SPI format

Data / Command is recognized with the first bit transferred at SDA. Data are transferred in the unit of 5 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 5 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 3-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

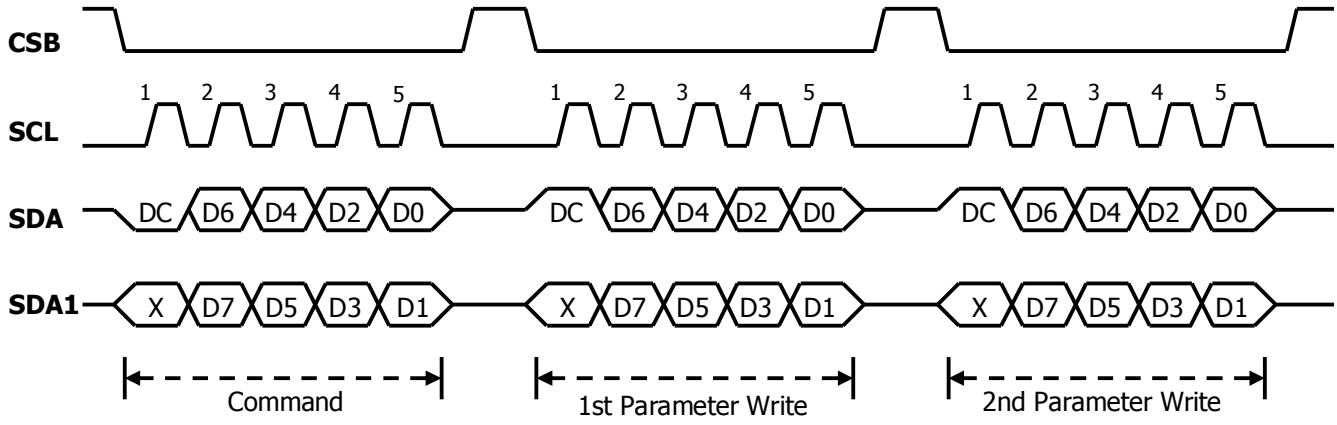


Figure: 3-wire dual SPI write operation

4 wire dual SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 4 SPI clocks. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 4 SPI clocks. (The serial counter is reset at the rising edge of the CSB signal.) In 4-wire dual SPI mode, SDA and SDA1 are only input mode for data write transmission.

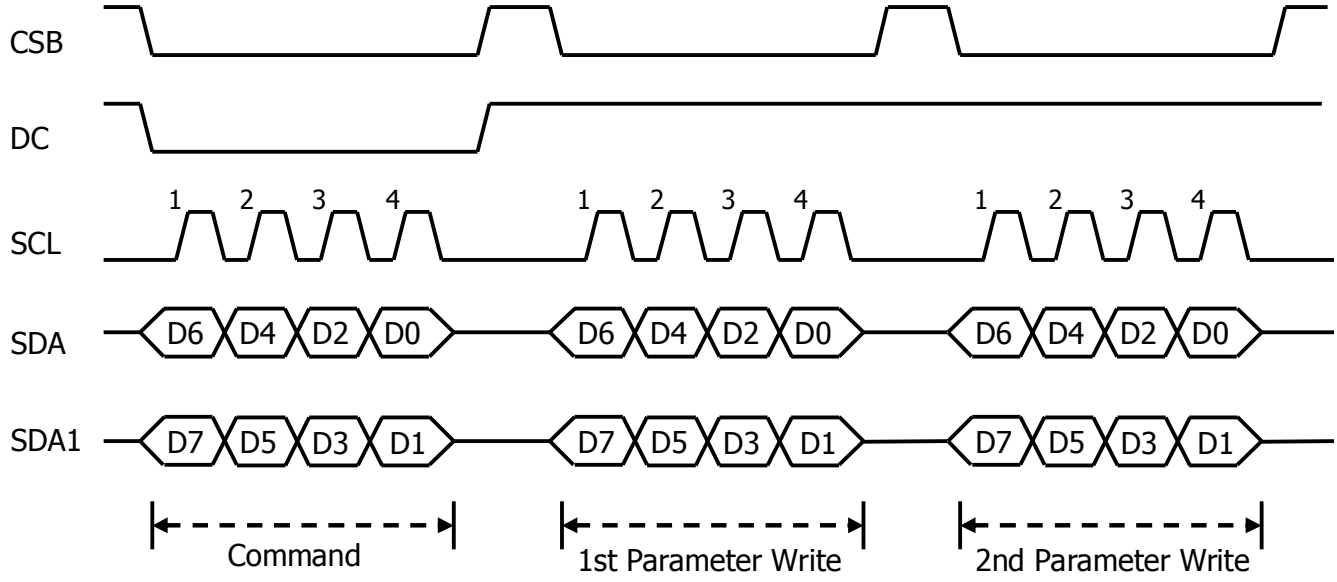
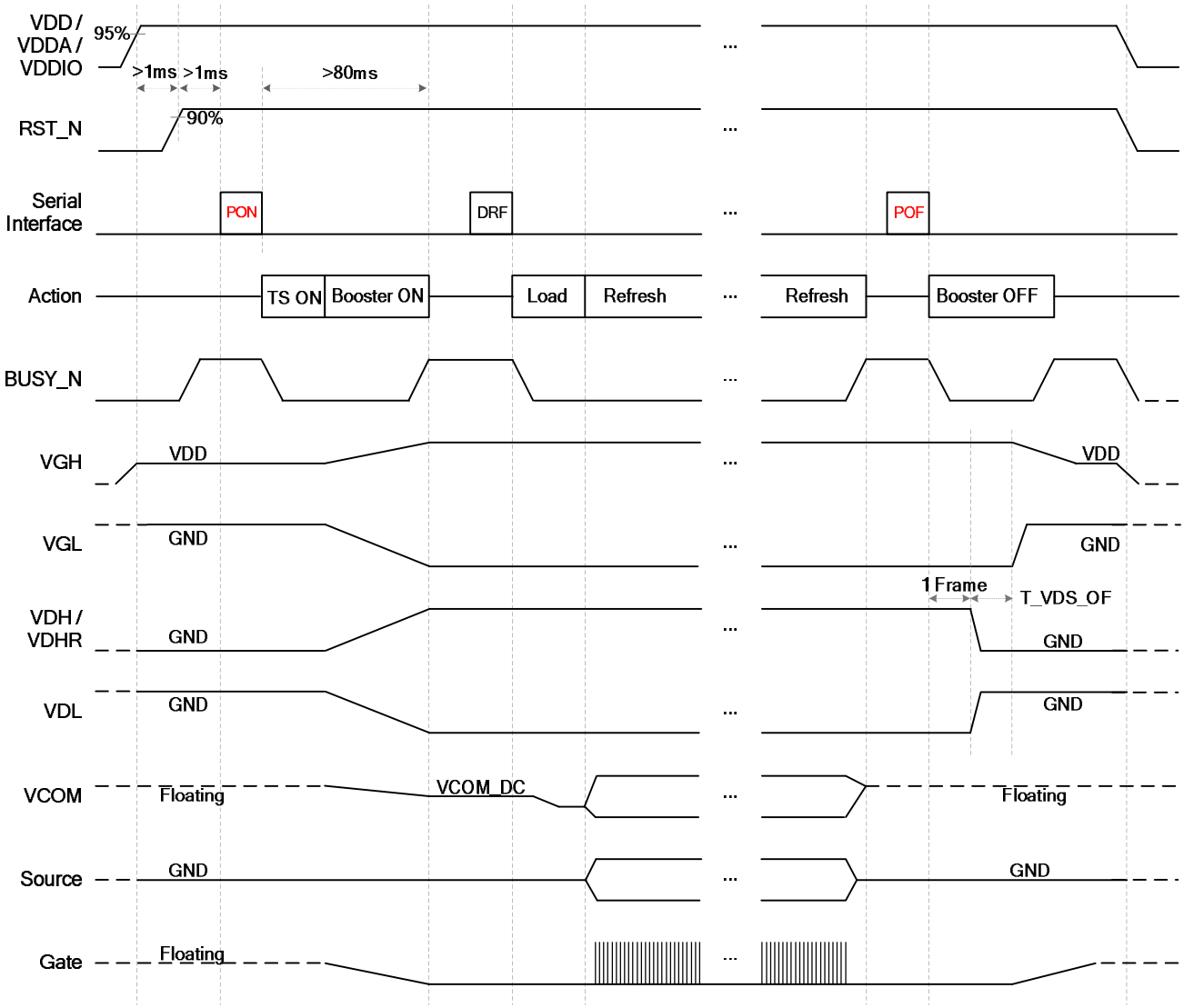


Figure: 4-wire dual SPI write operation

POWER MANAGEMENT

Power ON/OFF Sequence

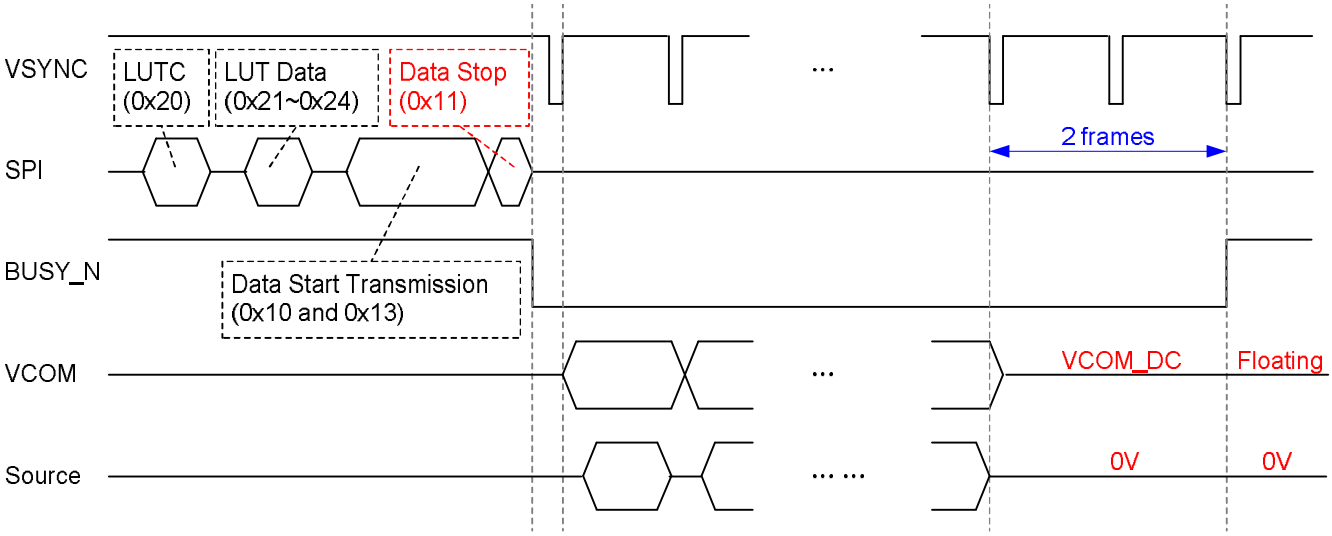
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



Data Transmission Waveform

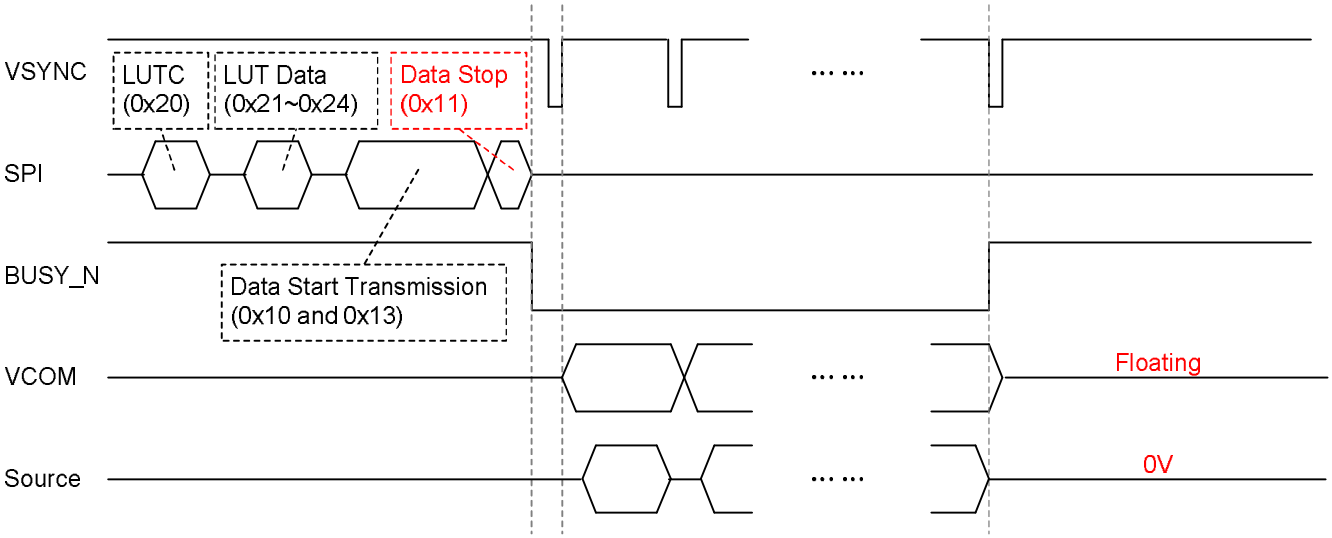
Example 1: After 3 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=0.
2. Meet the state whose Times to Repeat =0 and VCEND=0
3. Meet the state whose all Number of Frames =0 and VCEND=0



Example2: After 4 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

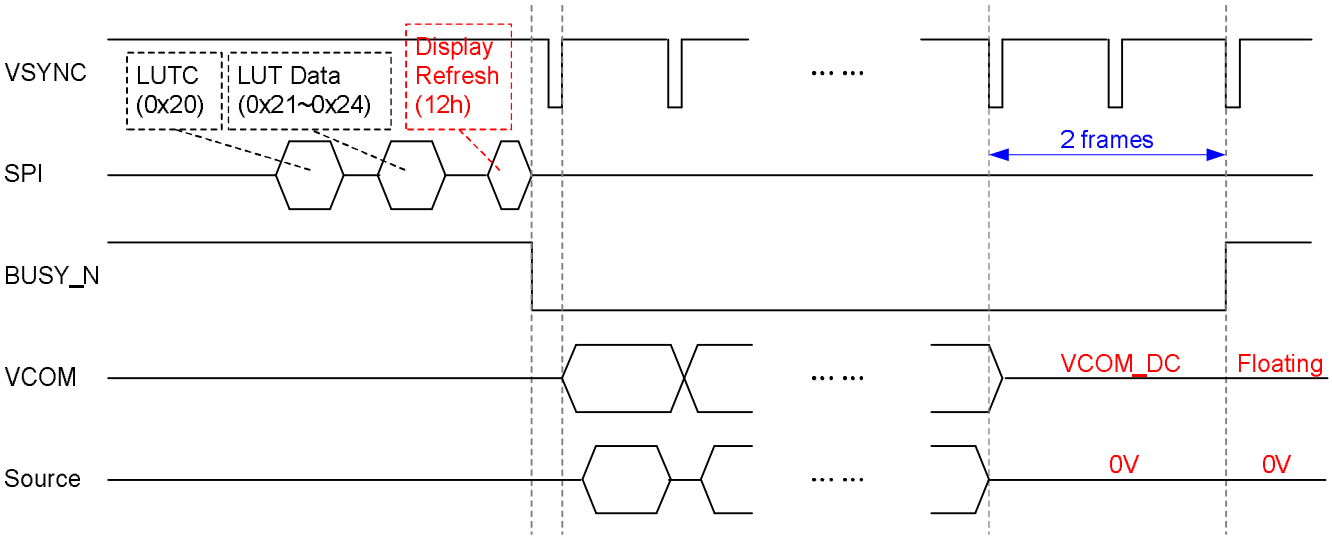
1. While level selection in LUT (LUTC only) is “1111_1111b”, all frame number are not ‘0’ and repeat times are not ‘0’, the driver will float VCOM.
2. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=1.
3. Meet the state whose Times to Repeat =0 and VCEND=1.
4. Meet the state whose all Number of Frames =0 and VCEND=1.



Display Refresh Waveform

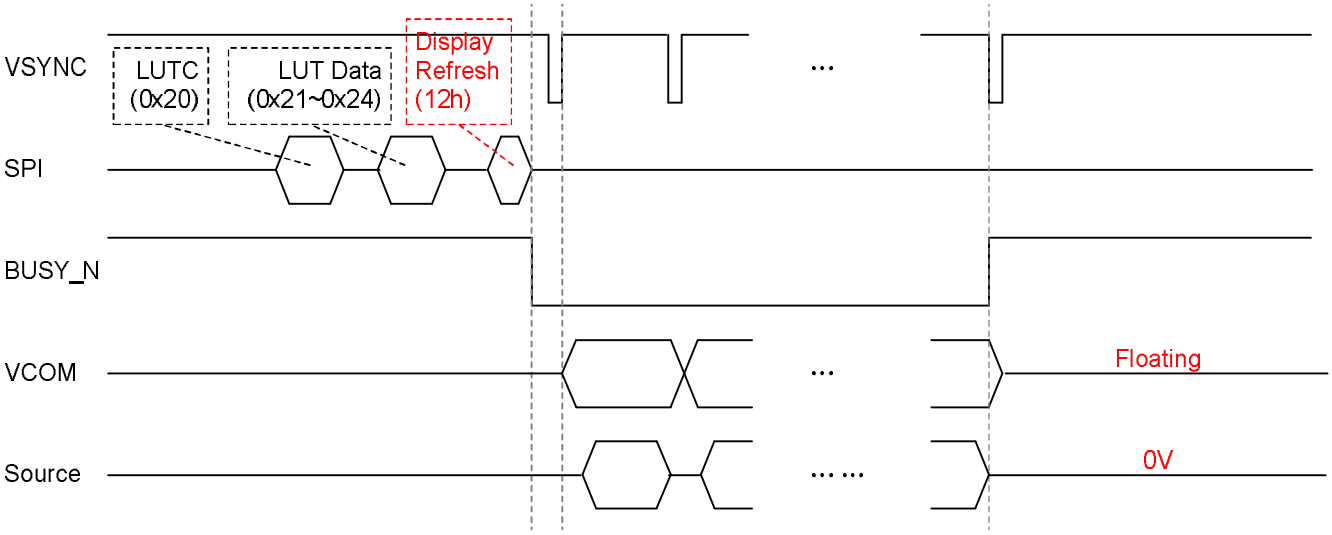
Example 1: After 3 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=0.
2. Meet the state whose Times to Repeat =0 and VCEND=0
3. Meet the state whose all Number of Frames =0 and VCEND=0



Example2: After 4 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. While level selection in LUT (LUTC only) is “1111_1111b”, all frame number are not ‘0’ and repeat times are not ‘0’, the driver will float VCOM.
2. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=1.
3. Meet the state whose Times to Repeat =0 and VCEND=1.
4. Meet the state whose all Number of Frames =0 and VCEND=1.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
DUSPI_EN	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTWB/LUTW	X	No action
LUTBW/LUTR	X	No action
LUTBB/LUTB	X	No action
LUTOPT	X	No action
KWOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
EVS	X	No action
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action
TSBDRY	X	No action

V: Accepted, X: Ignored

OTP Address Mapping

The size of the internal One Time Programmable (OTP) memory is 6K bytes, and the address is from 0x000 to 0x17FF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 can't be changed to logic 1.There is one area (0x0BF0~0x0BFF) reserved for Waveshare only. Write all 0xFF of data to skip the area. The recommended voltage of VPP during programming is 7.75V. In conditions other than programming, let VPP float or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 3K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x0000 and 0x0C00). The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x0000	Check Code (0xA5)	0x0C00	Check Code (0xA5)
0x0001	Temperature Boundary 0 (TB0)	0x0C01	Temperature Boundary 0 (TB0)
0x0002	Temperature Boundary 1 (TB1)	0x0C02	Temperature Boundary 1 (TB1)
0x0003	Temperature Boundary 2 (TB2)	0x0C03	Temperature Boundary 2 (TB2)
0x0004	Temperature Boundary 3 (TB3)	0x0C04	Temperature Boundary 3 (TB3)
0x0005	Temperature Boundary 4 (TB4)	0x0C05	Temperature Boundary 4 (TB4)
0x0006	Temperature Boundary 5 (TB5)	0x0C06	Temperature Boundary 5 (TB5)
0x0007	Temperature Boundary 6 (TB6)	0x0C07	Temperature Boundary 6 (TB6)
0x0008	Temperature Boundary 7 (TB7)	0x0C08	Temperature Boundary 7 (TB7)
0x0009	Temperature Boundary 8 (TB8)	0x0C09	Temperature Boundary 8 (TB8)
0x000A	Temperature Boundary 9 (TB9)	0x0C0A	Temperature Boundary 9 (TB9)
0x000B	Temperature Boundary 10 (TB10)	0x0C0B	Temperature Boundary 10 (TB10)
0x000C~0x001E	Command Defatult Setting (Note 1)	0x0C0C~0x0C1E	Command Defatult Setting (Note 1)
0x001F~0x0048	Border LUT	0x0C1F~0x0C48	Border LUT
0x0049~0x013F	TR0 (Note 2)	0x0C49~0x0D3F	TR0 (Note 2)
0x0140~0x0236	TR1 (Note 2)	0x0D40~0x0E36	TR1 (Note 2)
0x0237~0x032D	TR2 (Note 2)	0x0E37~0x0F2D	TR2 (Note 2)
0x032E~0x0424	TR3 (Note 2)	0x0F2E~0x1024	TR3 (Note 2)
0x0425~0x051B	TR4 (Note 2)	0x1025~0x111B	TR4 (Note 2)
0x051C~0x0612	TR5 (Note 2)	0x111C~0x1212	TR5 (Note 2)
0x0613~0x0709	TR6 (Note 2)	0x1213~0x1309	TR6 (Note 2)
0x070A~0x0800	TR7 (Note 2)	0x130A~0x1400	TR7 (Note 2)
0x0801~0x08F7	TR8 (Note 2)	0x1401~0x14F7	TR8 (Note 2)
0x08F8~0x09EE	TR9 (Note 2)	0x14F8~0x15EE	TR9 (Note 2)
0x09EF~0x0AE5	TR10 (Note 2)	0x15EF~0x16E5	TR10 (Note 2)
0x0AE6~0x0BDC	TR11 (Note 2)	0x16E6~0x17DC	TR11 (Note 2)
0x0BDD~0x0BDF	Production Version[23:0]	0x17DD~0x17DF	Production Version[23:0]
0x0BE0~0x0BE2	LUT Version[23:0]	0x17E0~0x17E2	LUT Version[23:0]
0x0BE3~0x0BEF	Blank (Note 3)	0x17E3~0x17FF	Blank (Note 3)
0x0BF0~0x0BFF	Reserved (Note 3)		

Note:

(1) See section "Command Default Setting" for more detail.

(2) See section "LUT Format in OTP" for more detail.

(3) "Blank" is available for user and "Reserved" is for Waveshare definition.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 11 temperature boundary settings (TBx) to determine 12 temperature ranges. The sequence of mechanism is from TB0 to TB10, as shown below. If less than 12 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x0000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1. Read 0x0C00	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x0001 / 0x0C01	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x0002 / 0x0C02	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x0003 / 0x0C03	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x0004 / 0x0C04	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x0005 / 0x0C05	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x0006 / 0x0C06	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x0007 / 0x0C07	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x0008 / 0x0C08	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x0009 / 0x0C09	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Read 0x000A / 0x0C0A	Real Temperature ≦ TB9	Use TR9's table & setting, exit
12. Read 0x000B / 0x0C0B	Real Temperature ≦ TB10	Use TR10's table & setting, exit
13. Other	Real Temperature > TB10	Use TR11's table & setting, finish

Note: TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 °C, TR0 is selected.

If temperature = -10 °C, TR1 is selected.

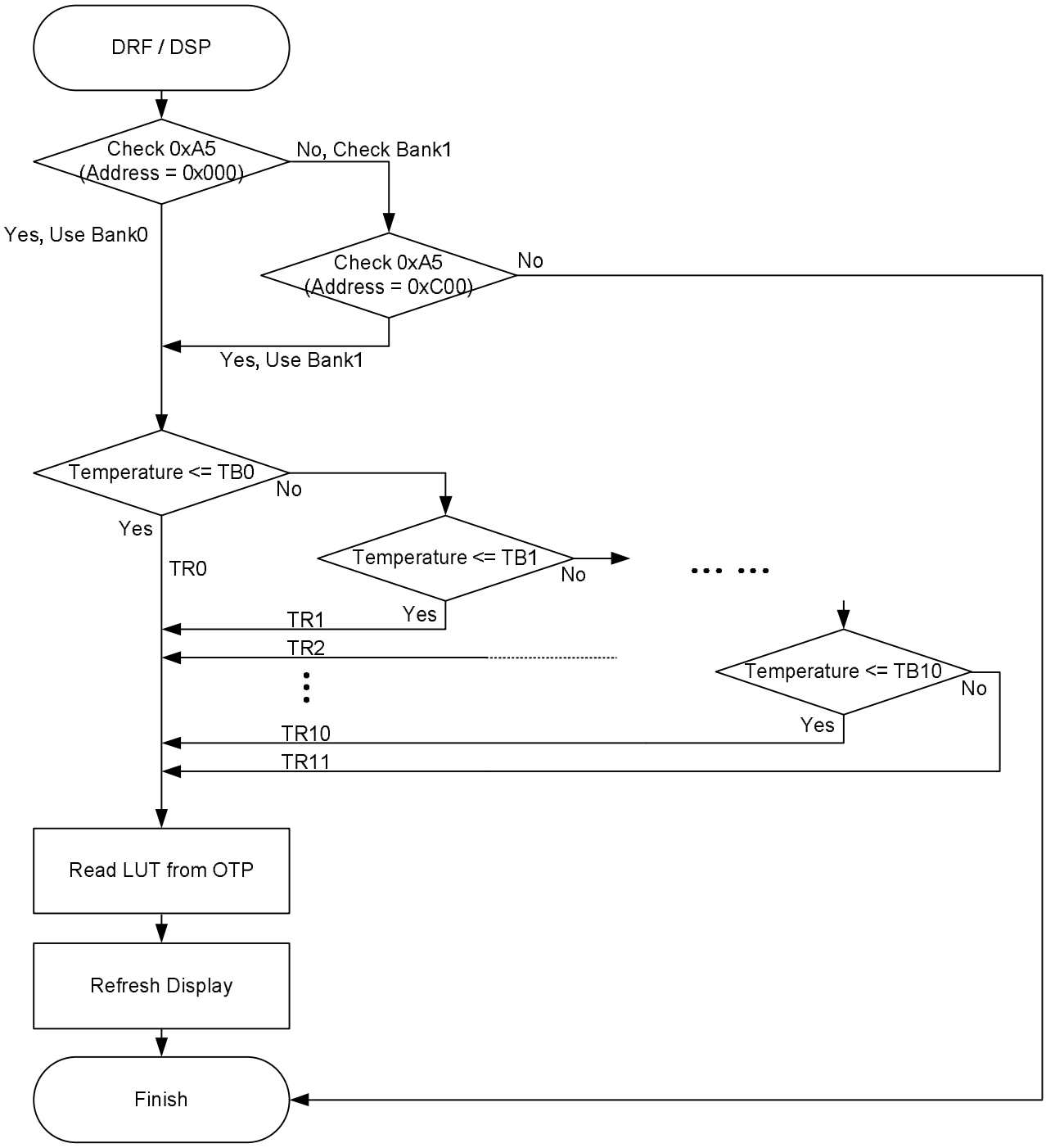
If temperature = 0 °C, TR2 is selected.

If temperature = 20 °C, TR4 is selected.

If temperature = 40 °C, TR5 is selected.

If temperature > 40 °C, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15 °C)
003h	0xFB	(-5 °C)
004h	0x00	(0 °C)
005h	0x0A	(10 °C)
006h	0x1E	(30 °C)
007h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x000C~0x001E (or 0x0C0C~0x0C1E). The data of address 0x000C (or 0x0C0C) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x000C	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x000D	--	--	#	#	#	#	--	--	PSR	REG, KW/R, UD, SHL	0x0F
0x000E	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x000F	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x0010	--	--	#	#	#	#	#	#		BT_PHC1[5:0]	0x17
0x0011	#	--	#	#	#	#	#	#		PHC2EN, BT_PHC2[5:0]	0x17
0x0012	--	--	--	--	--	--	#	#	KWOPT	ATRED, NORED	0x00
0x0013	#	--	#	#	#	--	#	#	CDI	BDZ, BDV[1:0], N2OCP, DDX[1:0]	0x31
0x0014	--	--	--	--	#	#	#	#		CDI[3:0]	0x07
0x0015	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x0016	--	#	#	#	#	#	#	#	TRES	HRES[9:3]	0x64
0x0017	--	--	--	--	--	--	#	#		VRES[9:0]	0x02
0x0018	#	#	#	#	#	#	#	#			0x58
0x0019	--	#	#	#	#	#	#	#	GSST	HST[9:3]	0x00
0x001A	--	--	--	--	--	--	#	#		VST[9:0]	0x00
0x001B	#	#	#	#	#	#	#	#			0x00
0x001C	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x001D	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x001E	#	#	#	#	#	#	#	#	TSBDRY	TSBDRY_PHC2[7:0]	0x00

LUT FORMAT IN OTP

There are 12 TRs (temperature range) in a bank. Each TR has independant frame rate, voltage, XON settings, KW option enable setting and LUTs. The fomat of LUT is different in different mode. In KWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTB in TRs. LUTC, LUTR, LUTW and LUTB have 10 states. In KW mode, there are 5 LUTs including LUT, LUTWW, LUTBW, LUTWB and LUTBB in TRs. All LUTs have 7 states. Besides, there is 1 common border LUT, regardless of temperature range, in KWR mode or KW mode.

Common Border LUT Table

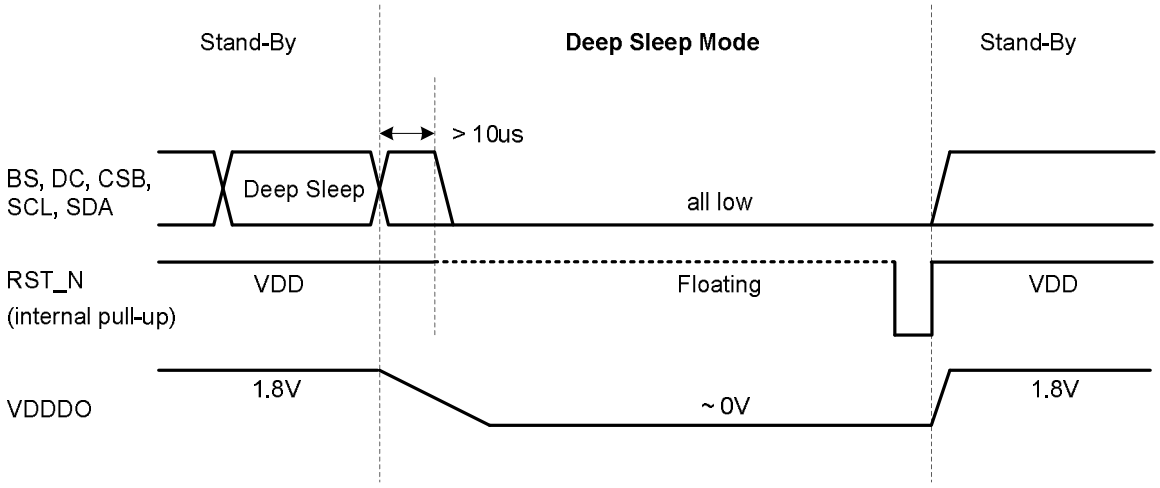
Common Border LUT Table	KWR Mode or KW Mode	
	Address (Bank0 / Bank1)	Content
	0x001F ~ 0x0048 / 0x0C1F ~ 0x0C48	LUTBD

Separate VCOM LUT and Source LUT (Example: Bank0 / TR0)

	KWR Mode (KW/R=0)		KW Mode (KW/R=1)	
	Address	Content	Address	Content
TR0	0x0049	Frame Rate[3:0], VCEND, VG Voltage[2:0]	0x0049	Frame Rate[3:0],VCEND,VG Voltage[2:0]
	0x004A	BDEND[1:0], VDH Voltage[5:0]	0x004A	BDEND[1:0], VDH Voltage[5:0]
	0x004B	XON[9:8], VDL Voltage [5:0]	0x004B	XON[9:8], VDL Voltage [5:0]
	0x004C	KWE[9:8], VDHR Voltage [5:0]	0x004C	KWE[9:8], VDHR Voltage [5:0]
	0x004D	XON [7:0]	0x004D	XON [7:0]
	0x004E	0b, VCOM_DC[6:0]	0x004E	0b, VCOM_DC[6:0]
	0x004F	KWE[7:0]	0x004F | 0x0078	LUTC (7 states)
	0x0050 | 0x008B	LUTC (10 states)	0x0079 | 0x00A2	LUTWW (7 states)
	0x008C | 0x00C7	LUTR (10 states)	0x00A3 | 0x00CC	LUTKW (7 states)
	0x00C8 | 0x0103	LUTW (10 states)	0x00CD | 0x00F6	LUTWK (7 states)
	0x0104 | 0x013F	LUTK (10 states)	0x00F7 | 0x0120	LUTKK (7 states)
			0x0121 | 0x013F	Reserved

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, WF8104 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

Figure: Panel break check layout example

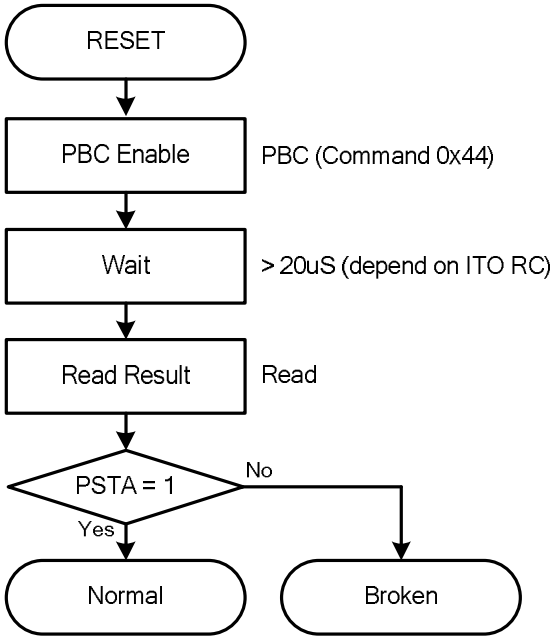
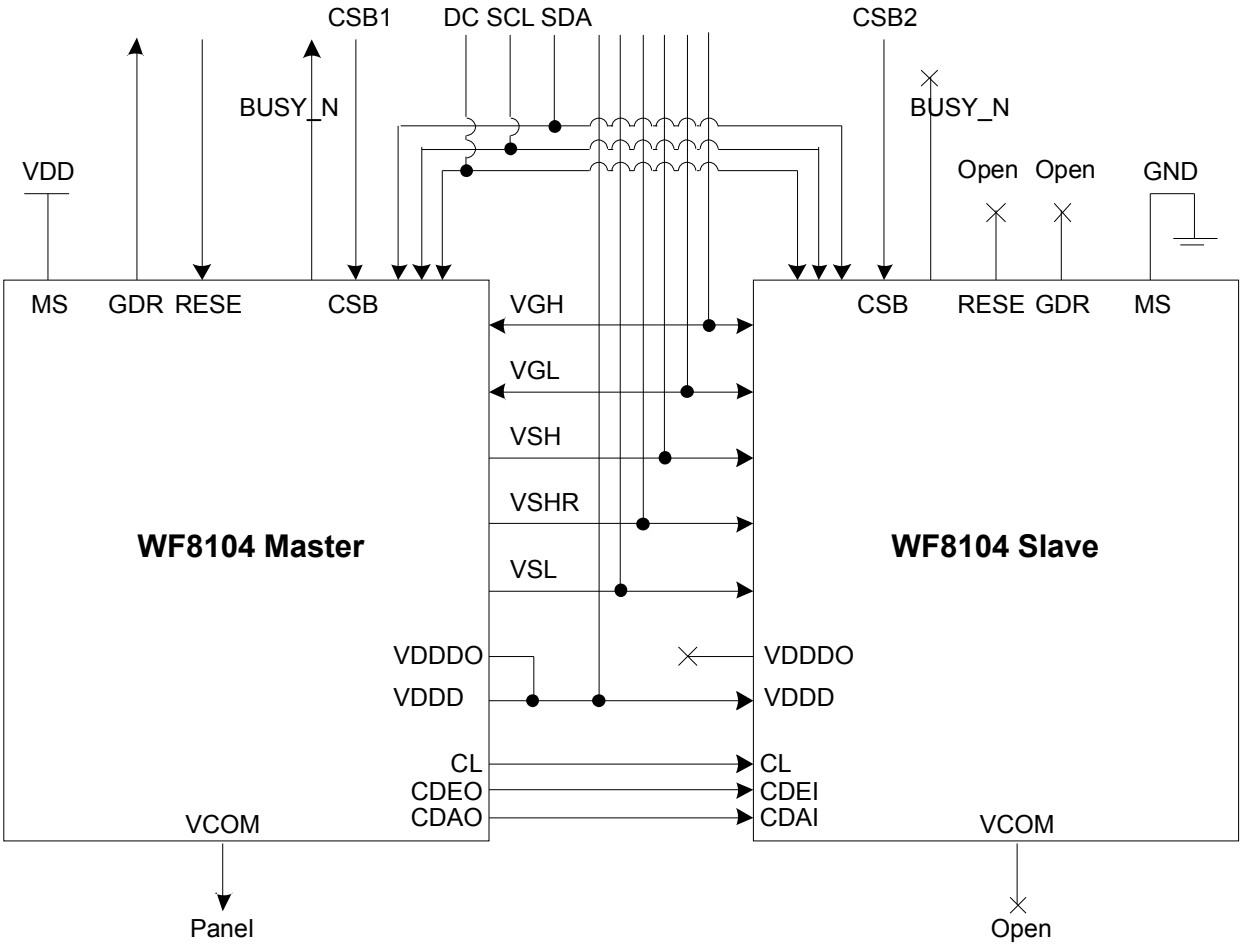


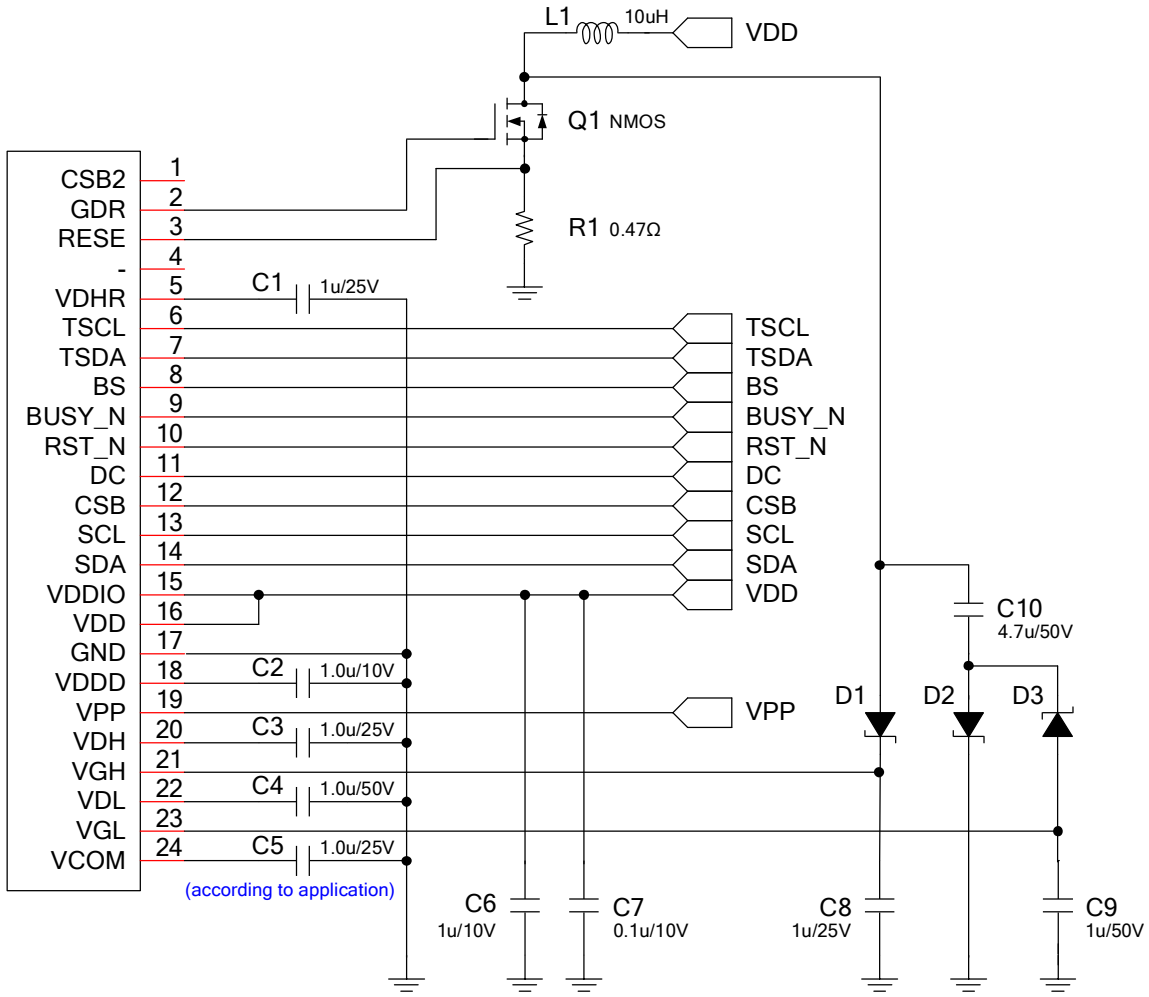
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT

All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.



BOOSTER APPLICATION CIRCUIT



Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 20V, I_D > 500mA, $V_{GS}(th)$ < 1.5V, C_{ISS} < 200pF, $R_{DS}(on)$ < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 20V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_A=100°C)

Recommended Resistor

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VDH, VDL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, SDA1, GDR, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDIO}, V_{DDA}	Logic Supply voltage	-0.3	+6.0	V
V_{PP}	OTP programming voltage	-0.3	+8.0	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VGH-VGL	Supply range	-	+44.0	V
Source				
VDH	Analog supply voltage – positive	+16		V
VDL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
IVGH	Input rush current for VGH	(TBD)	(TBD)	mA
IVGL	Input rush current for VGL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
V_{DDIO}	IO supply voltage		2.3	3.3	3.6	V
V_{DD}	Supply voltage		2.3	3.3	3.6	V
V_{DDA}	DCDC driver supply voltage		2.3	3.3	3.6	V
V_{IL}	LOW Level input voltage	Digital input pins	0	--	0.3xV_{DD}	V
V_{IH}	HIGH Level input voltage	Digital input pins	0.7xV_{DDIO}	--	V_{DDIO}	V
V_{OH}	HIGH Level output voltage	Digital input pins, I_{OH}=400uA	V_{DDIO}-0.4	--	--	V
V_{OL}	LOW Level Output voltage	Digital input pins, I_{OL}=-400uA	0	--	0.4	V
I_{IN}	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
R_{IN}	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVDH	Supply voltage dev		-200	0	+200	mV
dVDL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
R_{ON}	Driver Output Resistance	For source driver, T_{OP}=25°C, V_{OUT} = ±15V For gate driver, T_{OP}=25°C, V_{OUT} = ±20V		16.0 4.0	38.4 8	KΩ

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
I_{VDD}	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
I_{VDDIO}	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
I_{VDDA}	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =126us VCOM DC No load	--	--	4.0	mA
		Source output VDH/VDL, Duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	--	20.0	

AC CHARACTERISTICS

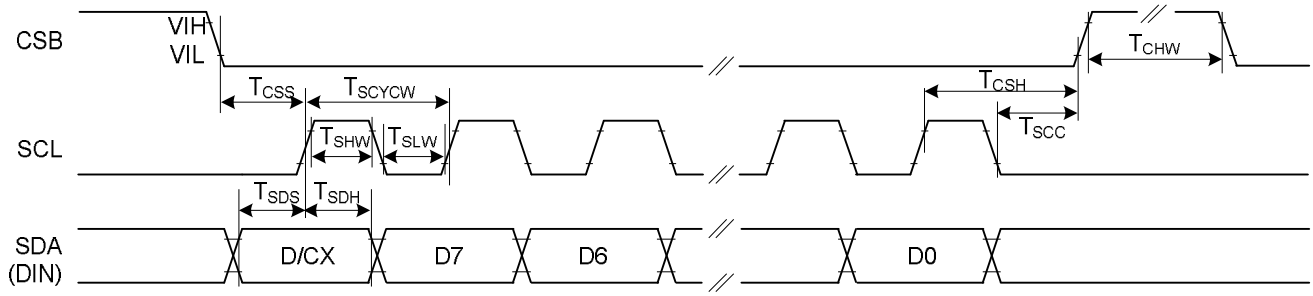


Figure: 3-wire Serial Interface Characteristics (Write mode)

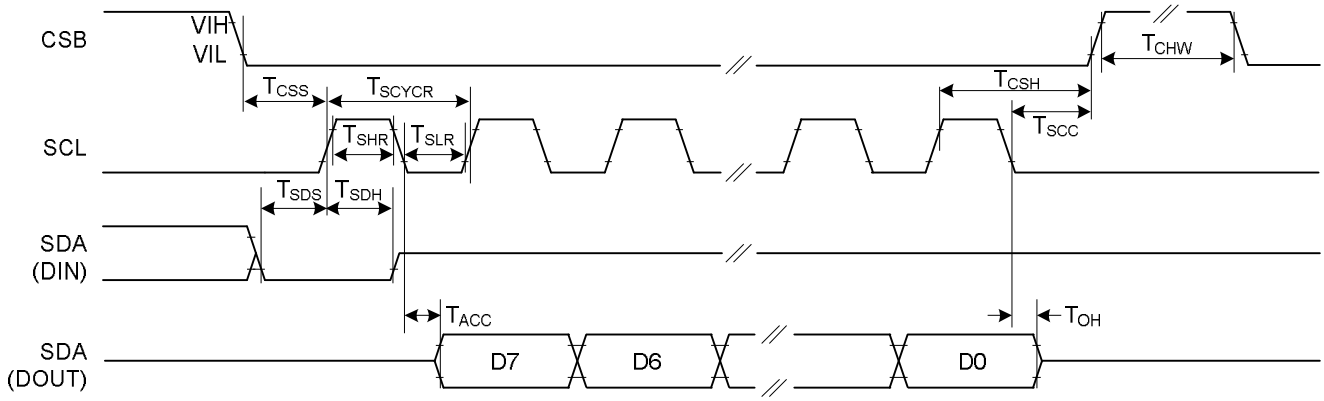


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

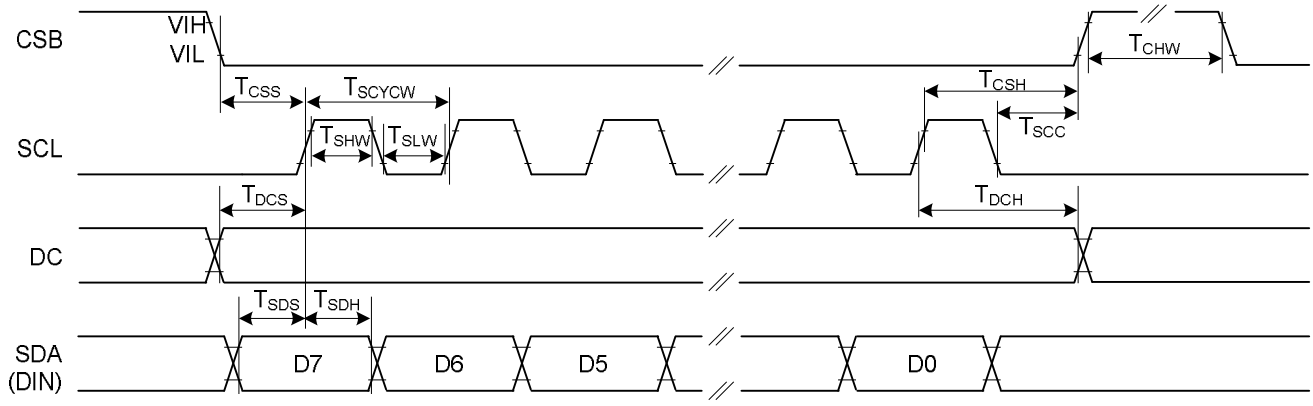


Figure: 4-wire Serial Interface Characteristics (Write mode)

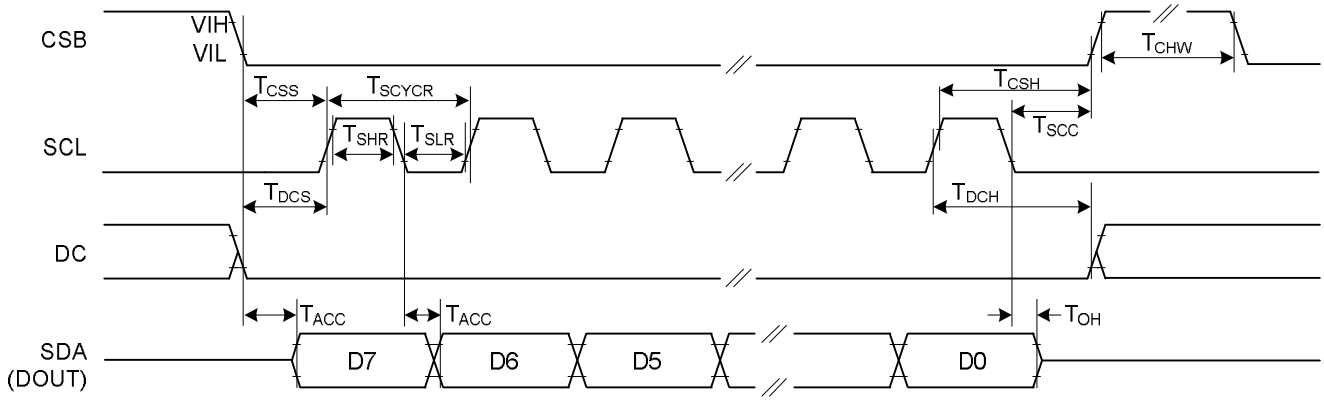
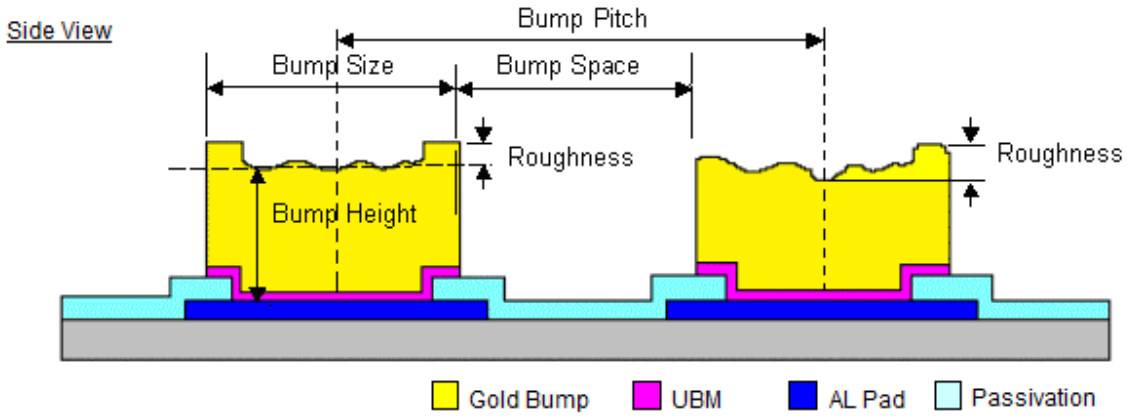


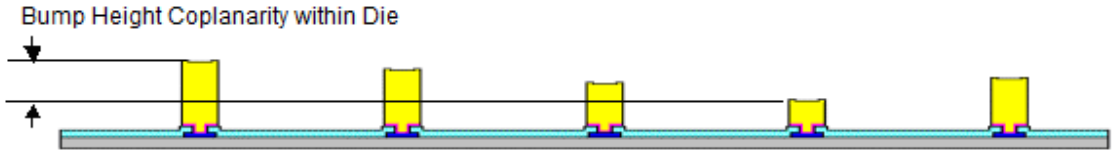
Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

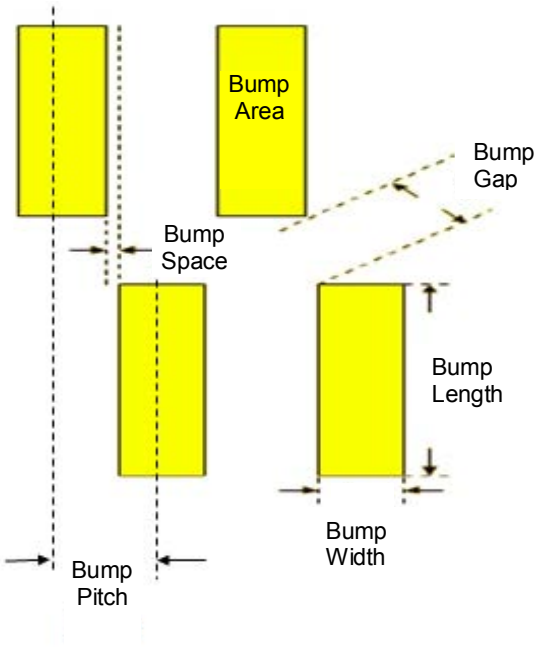
PHYSICAL DIMENSIONS

Die Size:	(18512 µM 6 40µM) x (1142 µM 6 40µM)
Die Thickness:	300 µM 6 20µM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2µM
Bump Height:	12 µM 6 3µM
	(H_{MAX} – H_{MIN}) within die ≤ 2µM
Bump Size:	12 µM x 100 µM 6 2µM
Bump Area:	1200 μM^2
Bump Pitch:	25 µM
Bump Gap:	19 µM 6 3µM
Hardness:	65 Hv 6 15Hv
Shear:	/ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center



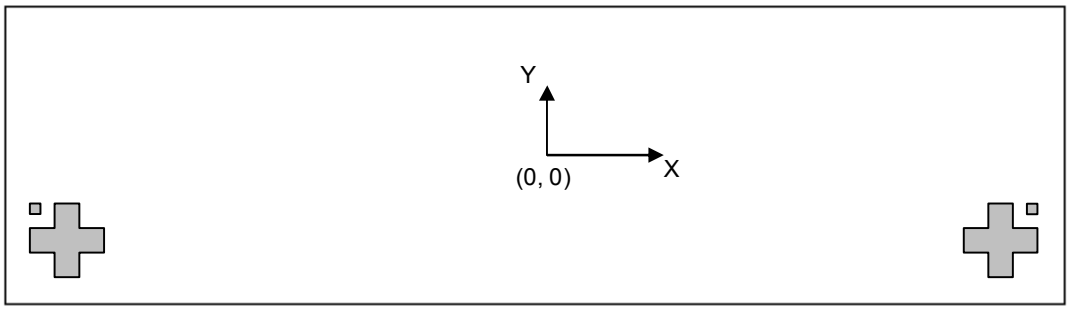


For Stagger Layout



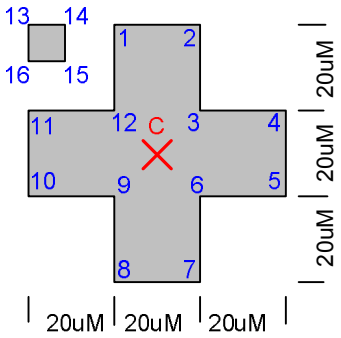
ALIGNMENT MARK INFORMATION

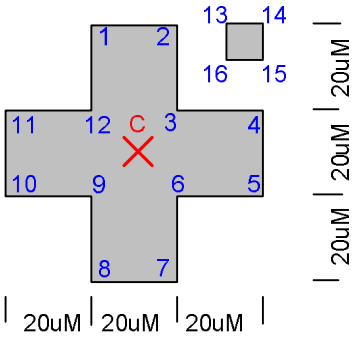
Location:



D-Left Mark D-Right Mark

Shapes and Points:





Point Coordinates:

	D-Left Mark		D-Right Mark	
Point	X	Y	X	Y
C (X)	-9183	-498	9183	-498
1	-9193	-468	9173	-468
2	-9173	-468	9193	-468
3	-9173	-488	9193	-488
4	-9153	-488	9213	-488
5	-9153	-508	9213	-508
6	-9173	-508	9193	-508
7	-9173	-528	9193	-528
8	-9193	-528	9173	-528
9	-9193	-508	9173	-508
10	-9213	-508	9153	-508
11	-9213	-488	9153	-488
12	-9193	-488	9173	-488
13	-9213	-468	9203	-468
14	-9203	-468	9213	-468
15	-9203	-478	9213	-478
16	-9213	-478	9203	-478

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-9062	-515	28	70
2	DUMMY	-9016	-515	28	70
3	VCOM	-8970	-515	28	70
4	VCOM	-8924	-515	28	70
5	VCOM	-8878	-515	28	70
6	VCOM	-8832	-515	28	70
7	VCOM	-8786	-515	28	70
8	VCOM	-8740	-515	28	70
9	VCOM	-8694	-515	28	70
10	VCOM	-8648	-515	28	70
11	VCOM	-8602	-515	28	70
12	VCOM	-8556	-515	28	70
13	VCOM	-8510	-515	28	70
14	VCOM	-8464	-515	28	70
15	VCOM	-8418	-515	28	70
16	VCOM	-8372	-515	28	70
17	VCOM	-8326	-515	28	70
18	VCOM	-8280	-515	28	70
19	VCOM	-8234	-515	28	70
20	VCOM	-8188	-515	28	70
21	VCOM	-8142	-515	28	70
22	VDM	-8096	-515	28	70
23	VGL	-8050	-515	28	70
24	VGL	-8004	-515	28	70
25	VGL	-7958	-515	28	70
26	VGL	-7912	-515	28	70
27	VGL	-7866	-515	28	70
28	VGL	-7820	-515	28	70
29	VGL	-7774	-515	28	70
30	VGL	-7728	-515	28	70
31	VGL	-7682	-515	28	70
32	VGL	-7636	-515	28	70
33	VGL	-7590	-515	28	70
34	VGL	-7544	-515	28	70
35	VGL	-7498	-515	28	70
36	VGL	-7452	-515	28	70
37	VDM	-7406	-515	28	70
38	VDL	-7360	-515	28	70
39	VDL	-7314	-515	28	70
40	VDL	-7268	-515	28	70
41	VDL	-7222	-515	28	70
42	VDL	-7176	-515	28	70
43	VDL	-7130	-515	28	70
44	VDL	-7084	-515	28	70
45	VDL	-7038	-515	28	70
46	VDL	-6992	-515	28	70
47	VDL	-6946	-515	28	70
48	VDL	-6900	-515	28	70
49	VDL	-6854	-515	28	70
50	GNDA	-6808	-515	28	70
51	VGH	-6762	-515	28	70
52	VGH	-6716	-515	28	70
53	VGH	-6670	-515	28	70
54	VGH	-6624	-515	28	70
55	VGH	-6578	-515	28	70
56	VGH	-6532	-515	28	70
57	VGH	-6486	-515	28	70

#	Pad	X	Y	W	H
58	VGH	-6440	-515	28	70
59	VGH	-6394	-515	28	70
60	VGH	-6348	-515	28	70
61	VGH	-6302	-515	28	70
62	VGH	-6256	-515	28	70
63	VGH	-6210	-515	28	70
64	VGH	-6164	-515	28	70
65	GNDA	-6118	-515	28	70
66	VDH	-6072	-515	28	70
67	VDH	-6026	-515	28	70
68	VDH	-5980	-515	28	70
69	VDH	-5934	-515	28	70
70	VDH	-5888	-515	28	70
71	VDH	-5842	-515	28	70
72	VDH	-5796	-515	28	70
73	VDH	-5750	-515	28	70
74	VDH	-5704	-515	28	70
75	VDH	-5658	-515	28	70
76	VDH	-5612	-515	28	70
77	VDH	-5566	-515	28	70
78	GNDA	-5520	-515	28	70
79	VPP	-5474	-515	28	70
80	VPP	-5428	-515	28	70
81	VPP	-5382	-515	28	70
82	VPP	-5336	-515	28	70
83	VPP	-5290	-515	28	70
84	VPP	-5244	-515	28	70
85	VPP	-5198	-515	28	70
86	VPP	-5152	-515	28	70
87	VPP	-5106	-515	28	70
88	VPP	-5060	-515	28	70
89	DUMMY	-5014	-515	28	70
90	DUMMY	-4968	-515	28	70
91	DUMMY	-4922	-515	28	70
92	DUMMY	-4876	-515	28	70
93	DUMMY	-4830	-515	28	70
94	DUMMY	-4784	-515	28	70
95	DUMMY	-4738	-515	28	70
96	DUMMY	-4692	-515	28	70
97	DUMMY	-4646	-515	28	70
98	DUMMY	-4600	-515	28	70
99	DUMMY	-4554	-515	28	70
100	DUMMY	-4508	-515	28	70
101	DUMMY	-4462	-515	28	70
102	DUMMY	-4416	-515	28	70
103	VDDDO	-4370	-515	28	70
104	VDDDO	-4324	-515	28	70
105	VDDDO	-4278	-515	28	70
106	VDDDO	-4232	-515	28	70
107	VDDDO	-4186	-515	28	70
108	VDDDO	-4140	-515	28	70
109	VDDDO	-4094	-515	28	70
110	VDDDO	-4048	-515	28	70
111	VDDD	-4002	-515	28	70
112	VDDD	-3956	-515	28	70
113	VDDD	-3910	-515	28	70
114	VDDD	-3864	-515	28	70

#	Pad	X	Y	W	H
115	VDDD	-3818	-515	28	70
116	VDDD	-3772	-515	28	70
117	VDDD	-3726	-515	28	70
118	VDDD	-3680	-515	28	70
119	GNDA	-3634	-515	28	70
120	GNDA	-3588	-515	28	70
121	GNDA	-3542	-515	28	70
122	GNDA	-3496	-515	28	70
123	GNDA	-3450	-515	28	70
124	GNDA	-3404	-515	28	70
125	GNDA	-3358	-515	28	70
126	GNDA	-3312	-515	28	70
127	GNDA	-3266	-515	28	70
128	GNDA	-3220	-515	28	70
129	GND	-3174	-515	28	70
130	GND	-3128	-515	28	70
131	GND	-3082	-515	28	70
132	GND	-3036	-515	28	70
133	GND	-2990	-515	28	70
134	GND	-2944	-515	28	70
135	GND	-2898	-515	28	70
136	GND	-2852	-515	28	70
137	GND	-2806	-515	28	70
138	GND	-2760	-515	28	70
139	VDM	-2714	-515	28	70
140	VDM	-2668	-515	28	70
141	VDM	-2622	-515	28	70
142	VDM	-2576	-515	28	70
143	VDD	-2530	-515	28	70
144	VDD	-2484	-515	28	70
145	VDD	-2438	-515	28	70
146	VDD	-2392	-515	28	70
147	VDD	-2346	-515	28	70
148	VDD	-2300	-515	28	70
149	VDD	-2254	-515	28	70
150	VDD	-2208	-515	28	70
151	VDD	-2162	-515	28	70
152	VDD	-2116	-515	28	70
153	VDDIO	-2070	-515	28	70
154	VDDIO	-2024	-515	28	70
155	VDDIO	-1978	-515	28	70
156	VDDIO	-1932	-515	28	70
157	VDDIO	-1886	-515	28	70
158	VDDIO	-1840	-515	28	70
159	VDDIO	-1794	-515	28	70
160	VDDIO	-1748	-515	28	70
161	VDDIO	-1702	-515	28	70
162	VDDIO	-1656	-515	28	70
163	VDDIO	-1610	-515	28	70
164	DUMMY	-1564	-515	28	70
165	DUMMY	-1518	-515	28	70
166	DUMMY	-1472	-515	28	70
167	DUMMY	-1426	-515	28	70
168	DUMMY	-1380	-515	28	70
169	DUMMY	-1334	-515	28	70
170	DUMMY	-1288	-515	28	70
171	DUMMY	-1242	-515	28	70
172	DUMMY	-1196	-515	28	70
173	DUMMY	-1150	-515	28	70
174	DUMMY	-1104	-515	28	70

#	Pad	X	Y	W	H
175	DUMMY	-1058	-515	28	70
176	DUMMY	-1012	-515	28	70
177	DUMMY	-966	-515	28	70
178	DUMMY	-920	-515	28	70
179	DUMMY	-874	-515	28	70
180	DUMMY	-828	-515	28	70
181	DUMMY	-782	-515	28	70
182	DUMMY	-736	-515	28	70
183	DUMMY	-690	-515	28	70
184	DUMMY	-644	-515	28	70
185	DUMMY	-598	-515	28	70
186	DUMMY	-552	-515	28	70
187	DUMMY	-506	-515	28	70
188	DUMMY	-460	-515	28	70
189	DUMMY	-414	-515	28	70
190	DUMMY	-368	-515	28	70
191	DUMMY	-322	-515	28	70
192	DUMMY	-276	-515	28	70
193	DUMMY	-230	-515	28	70
194	DUMMY	-184	-515	28	70
195	M2M1_SYNC	-138	-515	28	70
196	M2M1_SYNC	-92	-515	28	70
197	M1M2_SYNC	-46	-515	28	70
198	M1M2_SYNC	0	-515	28	70
199	LSYNC	46	-515	28	70
200	LSYNC	92	-515	28	70
201	MM	138	-515	28	70
202	MM	184	-515	28	70
203	DUMMY	230	-515	28	70
204	DUMMY	276	-515	28	70
205	DUMMY	322	-515	28	70
206	DUMMY	368	-515	28	70
207	DUMMY	414	-515	28	70
208	DUMMY	460	-515	28	70
209	DUMMY	506	-515	28	70
210	DUMMY	552	-515	28	70
211	VDDA	598	-515	28	70
212	VDDA	644	-515	28	70
213	VDDA	690	-515	28	70
214	VDDA	736	-515	28	70
215	VDDA	782	-515	28	70
216	VDDA	828	-515	28	70
217	VDDA	874	-515	28	70
218	VDDA	920	-515	28	70
219	VDDA	966	-515	28	70
220	VDDA	1012	-515	28	70
221	VDDA	1058	-515	28	70
222	VDDA	1104	-515	28	70
223	VDDA	1150	-515	28	70
224	SDA1	1196	-515	28	70
225	SDA1	1242	-515	28	70
226	SDA	1288	-515	28	70
227	SDA	1334	-515	28	70
228	SCL	1380	-515	28	70
229	SCL	1426	-515	28	70
230	GND	1472	-515	28	70
231	CSB	1518	-515	28	70
232	CSB	1564	-515	28	70
233	VDDIO	1610	-515	28	70
234	DUMMY	1656	-515	28	70

#	Pad	X	Y	W	H
235	DUMMY	1702	-515	28	70
236	GND	1748	-515	28	70
237	DC	1794	-515	28	70
238	DC	1840	-515	28	70
239	VDDIO	1886	-515	28	70
240	DUMMY	1932	-515	28	70
241	DUMMY	1978	-515	28	70
242	RST_N	2024	-515	28	70
243	RST_N	2070	-515	28	70
244	BUSY_N	2116	-515	28	70
245	BUSY_N	2162	-515	28	70
246	GND	2208	-515	28	70
247	DUMMY	2254	-515	28	70
248	DUMMY	2300	-515	28	70
249	DUMMY	2346	-515	28	70
250	CL	2392	-515	28	70
251	CL	2438	-515	28	70
252	CDEO	2484	-515	28	70
253	CDEO	2530	-515	28	70
254	CDAO	2576	-515	28	70
255	CDAO	2622	-515	28	70
256	CDAI	2668	-515	28	70
257	CDAI	2714	-515	28	70
258	CDEI	2760	-515	28	70
259	CDEI	2806	-515	28	70
260	GND	2852	-515	28	70
261	HSYNC	2898	-515	28	70
262	HSYNC	2944	-515	28	70
263	VDDIO	2990	-515	28	70
264	VSYNC	3036	-515	28	70
265	VSYNC	3082	-515	28	70
266	GND	3128	-515	28	70
267	DUMMY	3174	-515	28	70
268	VDDIO	3220	-515	28	70
269	BS	3266	-515	28	70
270	BS	3312	-515	28	70
271	GND	3358	-515	28	70
272	DUMMY	3404	-515	28	70
273	VDDIO	3450	-515	28	70
274	CHKGI	3496	-515	28	70
275	CHKGI	3542	-515	28	70
276	GND	3588	-515	28	70
277	MS	3634	-515	28	70
278	MS	3680	-515	28	70
279	VDDIO	3726	-515	28	70
280	GND	3772	-515	28	70
281	TSDA	3818	-515	28	70
282	TSDA	3864	-515	28	70
283	VDDIO	3910	-515	28	70
284	TSCL	3956	-515	28	70
285	TSCL	4002	-515	28	70
286	GND	4048	-515	28	70
287	CHKGO	4094	-515	28	70
288	CHKGO	4140	-515	28	70
289	DUMMY	4186	-515	28	70
290	DUMMY	4232	-515	28	70
291	DUMMY	4278	-515	28	70
292	DUMMY	4324	-515	28	70
293	DUMMY	4370	-515	28	70
294	DUMMY	4416	-515	28	70

#	Pad	X	Y	W	H
295	TEST13	4462	-515	28	70
296	TEST13	4508	-515	28	70
297	TEST12	4554	-515	28	70
298	TEST12	4600	-515	28	70
299	TEST11	4646	-515	28	70
300	TEST11	4692	-515	28	70
301	TEST10	4738	-515	28	70
302	TEST10	4784	-515	28	70
303	TEST9	4830	-515	28	70
304	TEST9	4876	-515	28	70
305	TEST8	4922	-515	28	70
306	TEST8	4968	-515	28	70
307	TEST7	5014	-515	28	70
308	TEST7	5060	-515	28	70
309	TEST6	5106	-515	28	70
310	TEST6	5152	-515	28	70
311	DUMMY	5198	-515	28	70
312	DUMMY	5244	-515	28	70
313	TEST5	5290	-515	28	70
314	TEST5	5336	-515	28	70
315	TEST4	5382	-515	28	70
316	TEST4	5428	-515	28	70
317	TEST3	5474	-515	28	70
318	TEST3	5520	-515	28	70
319	TEST2	5566	-515	28	70
320	TEST2	5612	-515	28	70
321	TEST1	5658	-515	28	70
322	TEST1	5704	-515	28	70
323	DUMMY	5750	-515	28	70
324	DUMMY	5796	-515	28	70
325	DUMMY	5842	-515	28	70
326	DUMMY	5888	-515	28	70
327	DUMMY	5934	-515	28	70
328	DUMMY	5980	-515	28	70
329	DUMMY	6026	-515	28	70
330	DUMMY	6072	-515	28	70
331	DUMMY	6118	-515	28	70
332	DUMMY	6164	-515	28	70
333	DUMMY	6210	-515	28	70
334	DUMMY	6256	-515	28	70
335	VDHR	6302	-515	28	70
336	VDHR	6348	-515	28	70
337	VDHR	6394	-515	28	70
338	VDHR	6440	-515	28	70
339	VDHR	6486	-515	28	70
340	VDHR	6532	-515	28	70
341	VDHR	6578	-515	28	70
342	VDHR	6624	-515	28	70
343	VDHR	6670	-515	28	70
344	VDHR	6716	-515	28	70
345	VDHR	6762	-515	28	70
346	VDHR	6808	-515	28	70
347	VDHR	6854	-515	28	70
348	VDHR	6900	-515	28	70
349	VDHR	6946	-515	28	70
350	VDHR	6992	-515	28	70
351	DUMMY	7038	-515	28	70
352	DUMMY	7084	-515	28	70
353	DUMMY	7130	-515	28	70
354	DUMMY	7176	-515	28	70

#	Pad	X	Y	W	H
355	DUMMY	7222	-515	28	70
356	DUMMY	7268	-515	28	70
357	GNDA	7314	-515	28	70
358	FB	7360	-515	28	70
359	FB	7406	-515	28	70
360	GNDA	7452	-515	28	70
361	RESE	7498	-515	28	70
362	RESE	7544	-515	28	70
363	RESE	7590	-515	28	70
364	RESE	7636	-515	28	70
365	VDM	7682	-515	28	70
366	GDR	7728	-515	28	70
367	GDR	7774	-515	28	70
368	GDR	7820	-515	28	70
369	GDR	7866	-515	28	70
370	GDR	7912	-515	28	70
371	GDR	7958	-515	28	70
372	GDR	8004	-515	28	70
373	GDR	8050	-515	28	70
374	GDR	8096	-515	28	70
375	GDR	8142	-515	28	70
376	GDR	8188	-515	28	70
377	GDR	8234	-515	28	70
378	GDR	8280	-515	28	70
379	GDR	8326	-515	28	70
380	VDM	8372	-515	28	70
381	VCOM	8418	-515	28	70
382	VCOM	8464	-515	28	70
383	VCOM	8510	-515	28	70
384	VCOM	8556	-515	28	70
385	VCOM	8602	-515	28	70
386	VCOM	8648	-515	28	70
387	VCOM	8694	-515	28	70
388	VCOM	8740	-515	28	70
389	VCOM	8786	-515	28	70
390	VCOM	8832	-515	28	70
391	VCOM	8878	-515	28	70
392	VCOM	8924	-515	28	70
393	VCOM	8970	-515	28	70
394	DUMMY	9016	-515	28	70
395	DUMMY	9062	-515	28	70
396	DUMMY	9169.5	500	12	100
397	DUMMY	9156.5	381	12	100
398	DUMMY	9144.5	500	12	100
399	GD<0>	9131.5	381	12	100
400	G<0>	9119.5	500	12	100
401	G<2>	9106.5	381	12	100
402	G<4>	9094.5	500	12	100
403	G<6>	9081.5	381	12	100
404	G<8>	9069.5	500	12	100
405	G<10>	9056.5	381	12	100
406	G<12>	9044.5	500	12	100
407	G<14>	9031.5	381	12	100
408	G<16>	9019.5	500	12	100
409	G<18>	9006.5	381	12	100
410	G<20>	8994.5	500	12	100
411	G<22>	8981.5	381	12	100
412	G<24>	8969.5	500	12	100
413	G<26>	8956.5	381	12	100
414	G<28>	8944.5	500	12	100

#	Pad	X	Y	W	H
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416	G<32>	8919.5	500	12	100
417	G<34>	8906.5	381	12	100
418	G<36>	8894.5	500	12	100
419	G<38>	8881.5	381	12	100
420	G<40>	8869.5	500	12	100
421	G<42>	8856.5	381	12	100
422	G<44>	8844.5	500	12	100
423	G<46>	8831.5	381	12	100
424	G<48>	8819.5	500	12	100
425	G<50>	8806.5	381	12	100
426	G<52>	8794.5	500	12	100
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429	G<58>	8756.5	381	12	100
430	G<60>	8744.5	500	12	100
431	G<62>	8731.5	381	12	100
432	G<64>	8719.5	500	12	100
433	G<66>	8706.5	381	12	100
434	G<68>	8694.5	500	12	100
435	G<70>	8681.5	381	12	100
436	G<72>	8669.5	500	12	100
437	G<74>	8656.5	381	12	100
438	G<76>	8644.5	500	12	100
439	G<78>	8631.5	381	12	100
440	G<80>	8619.5	500	12	100
441	G<82>	8606.5	381	12	100
442	G<84>	8594.5	500	12	100
443	G<86>	8581.5	381	12	100
444	G<88>	8569.5	500	12	100
445	G<90>	8556.5	381	12	100
446	G<92>	8544.5	500	12	100
447	G<94>	8531.5	381	12	100
448	G<96>	8519.5	500	12	100
449	G<98>	8506.5	381	12	100
450	G<100>	8494.5	500	12	100
451	G<102>	8481.5	381	12	100
452	G<104>	8469.5	500	12	100
453	G<106>	8456.5	381	12	100
454	G<108>	8444.5	500	12	100
455	G<110>	8431.5	381	12	100
456	G<112>	8419.5	500	12	100
457	G<114>	8406.5	381	12	100
458	G<116>	8394.5	500	12	100
459	G<118>	8381.5	381	12	100
460	G<120>	8369.5	500	12	100
461	G<122>	8356.5	381	12	100
462	G<124>	8344.5	500	12	100
463	G<126>	8331.5	381	12	100
464	G<128>	8319.5	500	12	100
465	G<130>	8306.5	381	12	100
466	G<132>	8294.5	500	12	100
467	G<134>	8281.5	381	12	100
468	G<136>	8269.5	500	12	100
469	G<138>	8256.5	381	12	100
470	G<140>	8244.5	500	12	100
471	G<142>	8231.5	381	12	100
472	G<144>	8219.5	500	12	100
473	G<146>	8206.5	381	12	100
474	G<148>	8194.5	500	12	100

#	Pad	X	Y	W	H
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476	G<152>	8169.5	500	12	100
477	G<154>	8156.5	381	12	100
478	G<156>	8144.5	500	12	100
479	G<158>	8131.5	381	12	100
480	G<160>	8119.5	500	12	100
481	G<162>	8106.5	381	12	100
482	G<164>	8094.5	500	12	100
483	G<166>	8081.5	381	12	100
484	G<168>	8069.5	500	12	100
485	G<170>	8056.5	381	12	100
486	G<172>	8044.5	500	12	100
487	G<174>	8031.5	381	12	100
488	G<176>	8019.5	500	12	100
489	G<178>	8006.5	381	12	100
490	G<180>	7994.5	500	12	100
491	G<182>	7981.5	381	12	100
492	G<184>	7969.5	500	12	100
493	G<186>	7956.5	381	12	100
494	G<188>	7944.5	500	12	100
495	G<190>	7931.5	381	12	100
496	G<192>	7919.5	500	12	100
497	G<194>	7906.5	381	12	100
498	G<196>	7894.5	500	12	100
499	G<198>	7881.5	381	12	100
500	G<200>	7869.5	500	12	100
501	G<202>	7856.5	381	12	100
502	G<204>	7844.5	500	12	100
503	G<206>	7831.5	381	12	100
504	G<208>	7819.5	500	12	100
505	G<210>	7806.5	381	12	100
506	G<212>	7794.5	500	12	100
507	G<214>	7781.5	381	12	100
508	G<216>	7769.5	500	12	100
509	G<218>	7756.5	381	12	100
510	G<220>	7744.5	500	12	100
511	G<222>	7731.5	381	12	100
512	G<224>	7719.5	500	12	100
513	G<226>	7706.5	381	12	100
514	G<228>	7694.5	500	12	100
515	G<230>	7681.5	381	12	100
516	G<232>	7669.5	500	12	100
517	G<234>	7656.5	381	12	100
518	G<236>	7644.5	500	12	100
519	G<238>	7631.5	381	12	100
520	G<240>	7619.5	500	12	100
521	G<242>	7606.5	381	12	100
522	G<244>	7594.5	500	12	100
523	G<246>	7581.5	381	12	100
524	G<248>	7569.5	500	12	100
525	G<250>	7556.5	381	12	100
526	G<252>	7544.5	500	12	100
527	G<254>	7531.5	381	12	100
528	G<256>	7519.5	500	12	100
529	G<258>	7506.5	381	12	100
530	G<260>	7494.5	500	12	100
531	G<262>	7481.5	381	12	100
532	G<264>	7469.5	500	12	100
533	G<266>	7456.5	381	12	100
534	G<268>	7444.5	500	12	100

#	Pad	X	Y	W	H
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536	G<272>	7419.5	500	12	100
537	G<274>	7406.5	381	12	100
538	G<276>	7394.5	500	12	100
539	G<278>	7381.5	381	12	100
540	G<280>	7369.5	500	12	100
541	G<282>	7356.5	381	12	100
542	G<284>	7344.5	500	12	100
543	G<286>	7331.5	381	12	100
544	G<288>	7319.5	500	12	100
545	G<290>	7306.5	381	12	100
546	G<292>	7294.5	500	12	100
547	G<294>	7281.5	381	12	100
548	G<296>	7269.5	500	12	100
549	G<298>	7256.5	381	12	100
550	G<300>	7244.5	500	12	100
551	G<302>	7231.5	381	12	100
552	G<304>	7219.5	500	12	100
553	G<306>	7206.5	381	12	100
554	G<308>	7194.5	500	12	100
555	G<310>	7181.5	381	12	100
556	G<312>	7169.5	500	12	100
557	G<314>	7156.5	381	12	100
558	G<316>	7144.5	500	12	100
559	G<318>	7131.5	381	12	100
560	G<320>	7119.5	500	12	100
561	G<322>	7106.5	381	12	100
562	G<324>	7094.5	500	12	100
563	G<326>	7081.5	381	12	100
564	G<328>	7069.5	500	12	100
565	G<330>	7056.5	381	12	100
566	G<332>	7044.5	500	12	100
567	G<334>	7031.5	381	12	100
568	G<336>	7019.5	500	12	100
569	G<338>	7006.5	381	12	100
570	G<340>	6994.5	500	12	100
571	G<342>	6981.5	381	12	100
572	G<344>	6969.5	500	12	100
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576	G<352>	6919.5	500	12	100
577	G<354>	6906.5	381	12	100
578	G<356>	6894.5	500	12	100
579	G<358>	6881.5	381	12	100
580	G<360>	6869.5	500	12	100
581	G<362>	6856.5	381	12	100
582	G<364>	6844.5	500	12	100
583	G<366>	6831.5	381	12	100
584	G<368>	6819.5	500	12	100
585	G<370>	6806.5	381	12	100
586	G<372>	6794.5	500	12	100
587	G<374>	6781.5	381	12	100
588	G<376>	6769.5	500	12	100
589	G<378>	6756.5	381	12	100
590	G<380>	6744.5	500	12	100
591	G<382>	6731.5	381	12	100
592	G<384>	6719.5	500	12	100
593	G<386>	6706.5	381	12	100
594	G<388>	6694.5	500	12	100

#	Pad	X	Y	W	H
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596	G<392>	6669.5	500	12	100
597	G<394>	6656.5	381	12	100
598	G<396>	6644.5	500	12	100
599	G<398>	6631.5	381	12	100
600	G<400>	6619.5	500	12	100
601	G<402>	6606.5	381	12	100
602	G<404>	6594.5	500	12	100
603	G<406>	6581.5	381	12	100
604	G<408>	6569.5	500	12	100
605	G<410>	6556.5	381	12	100
606	G<412>	6544.5	500	12	100
607	G<414>	6531.5	381	12	100
608	G<416>	6519.5	500	12	100
609	G<418>	6506.5	381	12	100
610	G<420>	6494.5	500	12	100
611	G<422>	6481.5	381	12	100
612	G<424>	6469.5	500	12	100
613	G<426>	6456.5	381	12	100
614	G<428>	6444.5	500	12	100
615	G<430>	6431.5	381	12	100
616	G<432>	6419.5	500	12	100
617	G<434>	6406.5	381	12	100
618	G<436>	6394.5	500	12	100
619	G<438>	6381.5	381	12	100
620	G<440>	6369.5	500	12	100
621	G<442>	6356.5	381	12	100
622	G<444>	6344.5	500	12	100
623	G<446>	6331.5	381	12	100
624	G<448>	6319.5	500	12	100
625	G<450>	6306.5	381	12	100
626	G<452>	6294.5	500	12	100
627	G<454>	6281.5	381	12	100
628	G<456>	6269.5	500	12	100
629	G<458>	6256.5	381	12	100
630	G<460>	6244.5	500	12	100
631	G<462>	6231.5	381	12	100
632	G<464>	6219.5	500	12	100
633	G<466>	6206.5	381	12	100
634	G<468>	6194.5	500	12	100
635	G<470>	6181.5	381	12	100
636	G<472>	6169.5	500	12	100
637	G<474>	6156.5	381	12	100
638	G<476>	6144.5	500	12	100
639	G<478>	6131.5	381	12	100
640	G<480>	6119.5	500	12	100
641	G<482>	6106.5	381	12	100
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653	G<506>	5956.5	381	12	100
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666	G<532>	5794.5	500	12	100
667	G<534>	5781.5	381	12	100
668	G<536>	5769.5	500	12	100
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672	G<544>	5719.5	500	12	100
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691	G<582>	5481.5	381	12	100
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717	S<10>	5063.5	381	12	100
718	S<11>	5050.5	500	12	100
719	S<12>	5037.5	381	12	100
720	S<13>	5024.5	500	12	100
721	S<14>	5011.5	381	12	100
722	S<15>	4998.5	500	12	100
723	S<16>	4985.5	381	12	100
724	S<17>	4972.5	500	12	100
725	S<18>	4959.5	381	12	100
726	S<19>	4946.5	500	12	100
727	S<20>	4933.5	381	12	100
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730	S<23>	4894.5	500	12	100
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732	S<25>	4868.5	500	12	100
733	S<26>	4855.5	381	12	100
734	S<27>	4842.5	500	12	100
735	S<28>	4829.5	381	12	100
736	S<29>	4816.5	500	12	100
737	S<30>	4803.5	381	12	100
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739	S<32>	4777.5	381	12	100
740	S<33>	4764.5	500	12	100
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745	S<38>	4699.5	381	12	100
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767	S<60>	4413.5	381	12	100
768	S<61>	4400.5	500	12	100
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770	S<63>	4374.5	500	12	100
771	S<64>	4361.5	381	12	100
772	S<65>	4348.5	500	12	100
773	S<66>	4335.5	381	12	100
774	S<67>	4322.5	500	12	100

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777	S<70>	4283.5	381	12	100
778	S<71>	4270.5	500	12	100
779	S<72>	4257.5	381	12	100
780	S<73>	4244.5	500	12	100
781	S<74>	4231.5	381	12	100
782	S<75>	4218.5	500	12	100
783	S<76>	4205.5	381	12	100
784	S<77>	4192.5	500	12	100
785	S<78>	4179.5	381	12	100
786	S<79>	4166.5	500	12	100
787	S<80>	4153.5	381	12	100
788	S<81>	4140.5	500	12	100
789	S<82>	4127.5	381	12	100
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791	S<84>	4101.5	381	12	100
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793	S<86>	4075.5	381	12	100
794	S<87>	4062.5	500	12	100
795	S<88>	4049.5	381	12	100
796	S<89>	4036.5	500	12	100
797	S<90>	4023.5	381	12	100
798	S<91>	4010.5	500	12	100
799	S<92>	3997.5	381	12	100
800	S<93>	3984.5	500	12	100
801	S<94>	3971.5	381	12	100
802	S<95>	3958.5	500	12	100
803	S<96>	3945.5	381	12	100
804	S<97>	3932.5	500	12	100
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808	S<101>	3880.5	500	12	100
809	S<102>	3867.5	381	12	100
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811	S<104>	3841.5	381	12	100
812	S<105>	3828.5	500	12	100
813	S<106>	3815.5	381	12	100
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817	S<110>	3763.5	381	12	100
818	S<111>	3750.5	500	12	100
819	S<112>	3737.5	381	12	100
820	S<113>	3724.5	500	12	100
821	S<114>	3711.5	381	12	100
822	S<115>	3698.5	500	12	100
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824	S<117>	3672.5	500	12	100
825	S<118>	3659.5	381	12	100
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828	S<121>	3620.5	500	12	100
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830	S<123>	3594.5	500	12	100
831	S<124>	3581.5	381	12	100
832	S<125>	3568.5	500	12	100
833	S<126>	3555.5	381	12	100
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838	S<131>	3490.5	500	12	100
839	S<132>	3477.5	381	12	100
840	S<133>	3464.5	500	12	100
841	S<134>	3451.5	381	12	100
842	S<135>	3438.5	500	12	100
843	S<136>	3425.5	381	12	100
844	S<137>	3412.5	500	12	100
845	S<138>	3399.5	381	12	100
846	S<139>	3386.5	500	12	100
847	S<140>	3373.5	381	12	100
848	S<141>	3360.5	500	12	100
849	S<142>	3347.5	381	12	100
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851	S<144>	3321.5	381	12	100
852	S<145>	3308.5	500	12	100
853	S<146>	3295.5	381	12	100
854	S<147>	3282.5	500	12	100
855	S<148>	3269.5	381	12	100
856	S<149>	3256.5	500	12	100
857	S<150>	3243.5	381	12	100
858	S<151>	3230.5	500	12	100
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862	S<155>	3178.5	500	12	100
863	S<156>	3165.5	381	12	100
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867	S<160>	3113.5	381	12	100
868	S<161>	3100.5	500	12	100
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871	S<164>	3061.5	381	12	100
872	S<165>	3048.5	500	12	100
873	S<166>	3035.5	381	12	100
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875	S<168>	3009.5	381	12	100
876	S<169>	2996.5	500	12	100
877	S<170>	2983.5	381	12	100
878	S<171>	2970.5	500	12	100
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884	S<177>	2892.5	500	12	100
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886	S<179>	2866.5	500	12	100
887	S<180>	2853.5	381	12	100
888	S<181>	2840.5	500	12	100
889	S<182>	2827.5	381	12	100
890	S<183>	2814.5	500	12	100
891	S<184>	2801.5	381	12	100
892	S<185>	2788.5	500	12	100
893	S<186>	2775.5	381	12	100
894	S<187>	2762.5	500	12	100

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897	S<190>	2723.5	381	12	100
898	S<191>	2710.5	500	12	100
899	S<192>	2697.5	381	12	100
900	S<193>	2684.5	500	12	100
901	S<194>	2671.5	381	12	100
902	S<195>	2658.5	500	12	100
903	S<196>	2645.5	381	12	100
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905	S<198>	2619.5	381	12	100
906	S<199>	2606.5	500	12	100
907	S<200>	2593.5	381	12	100
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910	S<203>	2554.5	500	12	100
911	S<204>	2541.5	381	12	100
912	S<205>	2528.5	500	12	100
913	S<206>	2515.5	381	12	100
914	S<207>	2502.5	500	12	100
915	S<208>	2489.5	381	12	100
916	S<209>	2476.5	500	12	100
917	S<210>	2463.5	381	12	100
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919	S<212>	2437.5	381	12	100
920	S<213>	2424.5	500	12	100
921	S<214>	2411.5	381	12	100
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924	S<217>	2372.5	500	12	100
925	S<218>	2359.5	381	12	100
926	S<219>	2346.5	500	12	100
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928	S<221>	2320.5	500	12	100
929	S<222>	2307.5	381	12	100
930	S<223>	2294.5	500	12	100
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932	S<225>	2268.5	500	12	100
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934	S<227>	2242.5	500	12	100
935	S<228>	2229.5	381	12	100
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941	S<234>	2151.5	381	12	100
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943	S<236>	2125.5	381	12	100
944	S<237>	2112.5	500	12	100
945	S<238>	2099.5	381	12	100
946	S<239>	2086.5	500	12	100
947	S<240>	2073.5	381	12	100
948	S<241>	2060.5	500	12	100
949	S<242>	2047.5	381	12	100
950	S<243>	2034.5	500	12	100
951	S<244>	2021.5	381	12	100
952	S<245>	2008.5	500	12	100
953	S<246>	1995.5	381	12	100
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957	S<250>	1943.5	381	12	100
958	S<251>	1930.5	500	12	100
959	S<252>	1917.5	381	12	100
960	S<253>	1904.5	500	12	100
961	S<254>	1891.5	381	12	100
962	S<255>	1878.5	500	12	100
963	S<256>	1865.5	381	12	100
964	S<257>	1852.5	500	12	100
965	S<258>	1839.5	381	12	100
966	S<259>	1826.5	500	12	100
967	S<260>	1813.5	381	12	100
968	S<261>	1800.5	500	12	100
969	S<262>	1787.5	381	12	100
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973	S<266>	1735.5	381	12	100
974	S<267>	1722.5	500	12	100
975	S<268>	1709.5	381	12	100
976	S<269>	1696.5	500	12	100
977	S<270>	1683.5	381	12	100
978	S<271>	1670.5	500	12	100
979	S<272>	1657.5	381	12	100
980	S<273>	1644.5	500	12	100
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982	S<275>	1618.5	500	12	100
983	S<276>	1605.5	381	12	100
984	S<277>	1592.5	500	12	100
985	S<278>	1579.5	381	12	100
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987	S<280>	1553.5	381	12	100
988	S<281>	1540.5	500	12	100
989	S<282>	1527.5	381	12	100
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991	S<284>	1501.5	381	12	100
992	S<285>	1488.5	500	12	100
993	S<286>	1475.5	381	12	100
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1001	S<294>	1371.5	381	12	100
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1004	S<297>	1332.5	500	12	100
1005	S<298>	1319.5	381	12	100
1006	S<299>	1306.5	500	12	100
1007	S<300>	1293.5	381	12	100
1008	S<301>	1280.5	500	12	100
1009	S<302>	1267.5	381	12	100
1010	S<303>	1254.5	500	12	100
1011	S<304>	1241.5	381	12	100
1012	S<305>	1228.5	500	12	100
1013	S<306>	1215.5	381	12	100
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1016	S<309>	1176.5	500	12	100
1017	S<310>	1163.5	381	12	100
1018	S<311>	1150.5	500	12	100
1019	S<312>	1137.5	381	12	100
1020	S<313>	1124.5	500	12	100
1021	S<314>	1111.5	381	12	100
1022	S<315>	1098.5	500	12	100
1023	S<316>	1085.5	381	12	100
1024	S<317>	1072.5	500	12	100
1025	S<318>	1059.5	381	12	100
1026	S<319>	1046.5	500	12	100
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1028	S<321>	1020.5	500	12	100
1029	S<322>	1007.5	381	12	100
1030	S<323>	994.5	500	12	100
1031	S<324>	981.5	381	12	100
1032	S<325>	968.5	500	12	100
1033	S<326>	955.5	381	12	100
1034	S<327>	942.5	500	12	100
1035	S<328>	929.5	381	12	100
1036	S<329>	916.5	500	12	100
1037	S<330>	903.5	381	12	100
1038	S<331>	890.5	500	12	100
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1040	S<333>	864.5	500	12	100
1041	S<334>	851.5	381	12	100
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1044	S<337>	812.5	500	12	100
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1053	S<346>	695.5	381	12	100
1054	S<347>	682.5	500	12	100
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1078	S<371>	370.5	500	12	100
1079	S<372>	357.5	381	12	100
1080	S<373>	344.5	500	12	100
1081	S<374>	331.5	381	12	100
1082	S<375>	318.5	500	12	100
1083	S<376>	305.5	381	12	100
1084	S<377>	292.5	500	12	100
1085	S<378>	279.5	381	12	100
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1090	S<383>	214.5	500	12	100
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1094	S<387>	162.5	500	12	100
1095	S<388>	149.5	381	12	100
1096	S<389>	136.5	500	12	100
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1098	S<391>	110.5	500	12	100
1099	S<392>	97.5	381	12	100
1100	S<393>	84.5	500	12	100
1101	S<394>	71.5	381	12	100
1102	S<395>	58.5	500	12	100
1103	S<396>	45.5	381	12	100
1104	S<397>	32.5	500	12	100
1105	S<398>	19.5	381	12	100
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1107	S<400>	-6.5	381	12	100
1108	S<401>	-19.5	500	12	100
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1111	S<404>	-58.5	381	12	100
1112	S<405>	-71.5	500	12	100
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1123	S<416>	-214.5	381	12	100
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1151	S<444>	-578.5	381	12	100
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1156	S<449>	-643.5	500	12	100
1157	S<450>	-656.5	381	12	100
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1160	S<453>	-695.5	500	12	100
1161	S<454>	-708.5	381	12	100
1162	S<455>	-721.5	500	12	100
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1166	S<459>	-773.5	500	12	100
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1172	S<465>	-851.5	500	12	100
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1174	S<467>	-877.5	500	12	100
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1187	S<480>	-1046.5	381	12	100
1188	S<481>	-1059.5	500	12	100
1189	S<482>	-1072.5	381	12	100
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1191	S<484>	-1098.5	381	12	100
1192	S<485>	-1111.5	500	12	100
1193	S<486>	-1124.5	381	12	100
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1198	S<491>	-1189.5	500	12	100
1199	S<492>	-1202.5	381	12	100
1200	S<493>	-1215.5	500	12	100
1201	S<494>	-1228.5	381	12	100
1202	S<495>	-1241.5	500	12	100
1203	S<496>	-1254.5	381	12	100
1204	S<497>	-1267.5	500	12	100
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1206	S<499>	-1293.5	500	12	100
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1208	S<501>	-1319.5	500	12	100
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1212	S<505>	-1371.5	500	12	100
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1214	S<507>	-1397.5	500	12	100
1215	S<508>	-1410.5	381	12	100
1216	S<509>	-1423.5	500	12	100
1217	S<510>	-1436.5	381	12	100
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1219	S<512>	-1462.5	381	12	100
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1228	S<521>	-1579.5	500	12	100
1229	S<522>	-1592.5	381	12	100
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1251	S<544>	-1878.5	381	12	100
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1253	S<546>	-1904.5	381	12	100
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1257	S<550>	-1956.5	381	12	100
1258	S<551>	-1969.5	500	12	100
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1260	S<553>	-1995.5	500	12	100
1261	S<554>	-2008.5	381	12	100
1262	S<555>	-2021.5	500	12	100
1263	S<556>	-2034.5	381	12	100
1264	S<557>	-2047.5	500	12	100
1265	S<558>	-2060.5	381	12	100
1266	S<559>	-2073.5	500	12	100
1267	S<560>	-2086.5	381	12	100
1268	S<561>	-2099.5	500	12	100
1269	S<562>	-2112.5	381	12	100
1270	S<563>	-2125.5	500	12	100
1271	S<564>	-2138.5	381	12	100
1272	S<565>	-2151.5	500	12	100
1273	S<566>	-2164.5	381	12	100
1274	S<567>	-2177.5	500	12	100
1275	S<568>	-2190.5	381	12	100
1276	S<569>	-2203.5	500	12	100
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1279	S<572>	-2242.5	381	12	100
1280	S<573>	-2255.5	500	12	100
1281	S<574>	-2268.5	381	12	100
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1283	S<576>	-2294.5	381	12	100
1284	S<577>	-2307.5	500	12	100
1285	S<578>	-2320.5	381	12	100
1286	S<579>	-2333.5	500	12	100
1287	S<580>	-2346.5	381	12	100
1288	S<581>	-2359.5	500	12	100
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1290	S<583>	-2385.5	500	12	100
1291	S<584>	-2398.5	381	12	100
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1298	S<591>	-2489.5	500	12	100
1299	S<592>	-2502.5	381	12	100
1300	S<593>	-2515.5	500	12	100
1301	S<594>	-2528.5	381	12	100
1302	S<595>	-2541.5	500	12	100
1303	S<596>	-2554.5	381	12	100
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1306	S<599>	-2593.5	500	12	100
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1311	S<604>	-2658.5	381	12	100
1312	S<605>	-2671.5	500	12	100
1313	S<606>	-2684.5	381	12	100
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1318	S<611>	-2749.5	500	12	100
1319	S<612>	-2762.5	381	12	100
1320	S<613>	-2775.5	500	12	100
1321	S<614>	-2788.5	381	12	100
1322	S<615>	-2801.5	500	12	100
1323	S<616>	-2814.5	381	12	100
1324	S<617>	-2827.5	500	12	100
1325	S<618>	-2840.5	381	12	100
1326	S<619>	-2853.5	500	12	100
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1328	S<621>	-2879.5	500	12	100
1329	S<622>	-2892.5	381	12	100
1330	S<623>	-2905.5	500	12	100
1331	S<624>	-2918.5	381	12	100
1332	S<625>	-2931.5	500	12	100
1333	S<626>	-2944.5	381	12	100
1334	S<627>	-2957.5	500	12	100
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1336	S<629>	-2983.5	500	12	100
1337	S<630>	-2996.5	381	12	100
1338	S<631>	-3009.5	500	12	100
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1340	S<633>	-3035.5	500	12	100
1341	S<634>	-3048.5	381	12	100
1342	S<635>	-3061.5	500	12	100
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1346	S<639>	-3113.5	500	12	100
1347	S<640>	-3126.5	381	12	100
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1352	S<645>	-3191.5	500	12	100
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1367	S<660>	-3386.5	381	12	100
1368	S<661>	-3399.5	500	12	100
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1370	S<663>	-3425.5	500	12	100
1371	S<664>	-3438.5	381	12	100
1372	S<665>	-3451.5	500	12	100
1373	S<666>	-3464.5	381	12	100
1374	S<667>	-3477.5	500	12	100

#	Pad	X	Y	W	H
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1381	S<674>	-3568.5	381	12	100
1382	S<675>	-3581.5	500	12	100
1383	S<676>	-3594.5	381	12	100
1384	S<677>	-3607.5	500	12	100
1385	S<678>	-3620.5	381	12	100
1386	S<679>	-3633.5	500	12	100
1387	S<680>	-3646.5	381	12	100
1388	S<681>	-3659.5	500	12	100
1389	S<682>	-3672.5	381	12	100
1390	S<683>	-3685.5	500	12	100
1391	S<684>	-3698.5	381	12	100
1392	S<685>	-3711.5	500	12	100
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1394	S<687>	-3737.5	500	12	100
1395	S<688>	-3750.5	381	12	100
1396	S<689>	-3763.5	500	12	100
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1398	S<691>	-3789.5	500	12	100
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1402	S<695>	-3841.5	500	12	100
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1404	S<697>	-3867.5	500	12	100
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1419	S<712>	-4062.5	381	12	100
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1425	S<718>	-4140.5	381	12	100
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1427	S<720>	-4166.5	381	12	100
1428	S<721>	-4179.5	500	12	100
1429	S<722>	-4192.5	381	12	100
1430	S<723>	-4205.5	500	12	100
1431	S<724>	-4218.5	381	12	100
1432	S<725>	-4231.5	500	12	100
1433	S<726>	-4244.5	381	12	100
1434	S<727>	-4257.5	500	12	100

#	Pad	X	Y	W	H
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1437	S<730>	-4296.5	381	12	100
1438	S<731>	-4309.5	500	12	100
1439	S<732>	-4322.5	381	12	100
1440	S<733>	-4335.5	500	12	100
1441	S<734>	-4348.5	381	12	100
1442	S<735>	-4361.5	500	12	100
1443	S<736>	-4374.5	381	12	100
1444	S<737>	-4387.5	500	12	100
1445	S<738>	-4400.5	381	12	100
1446	S<739>	-4413.5	500	12	100
1447	S<740>	-4426.5	381	12	100
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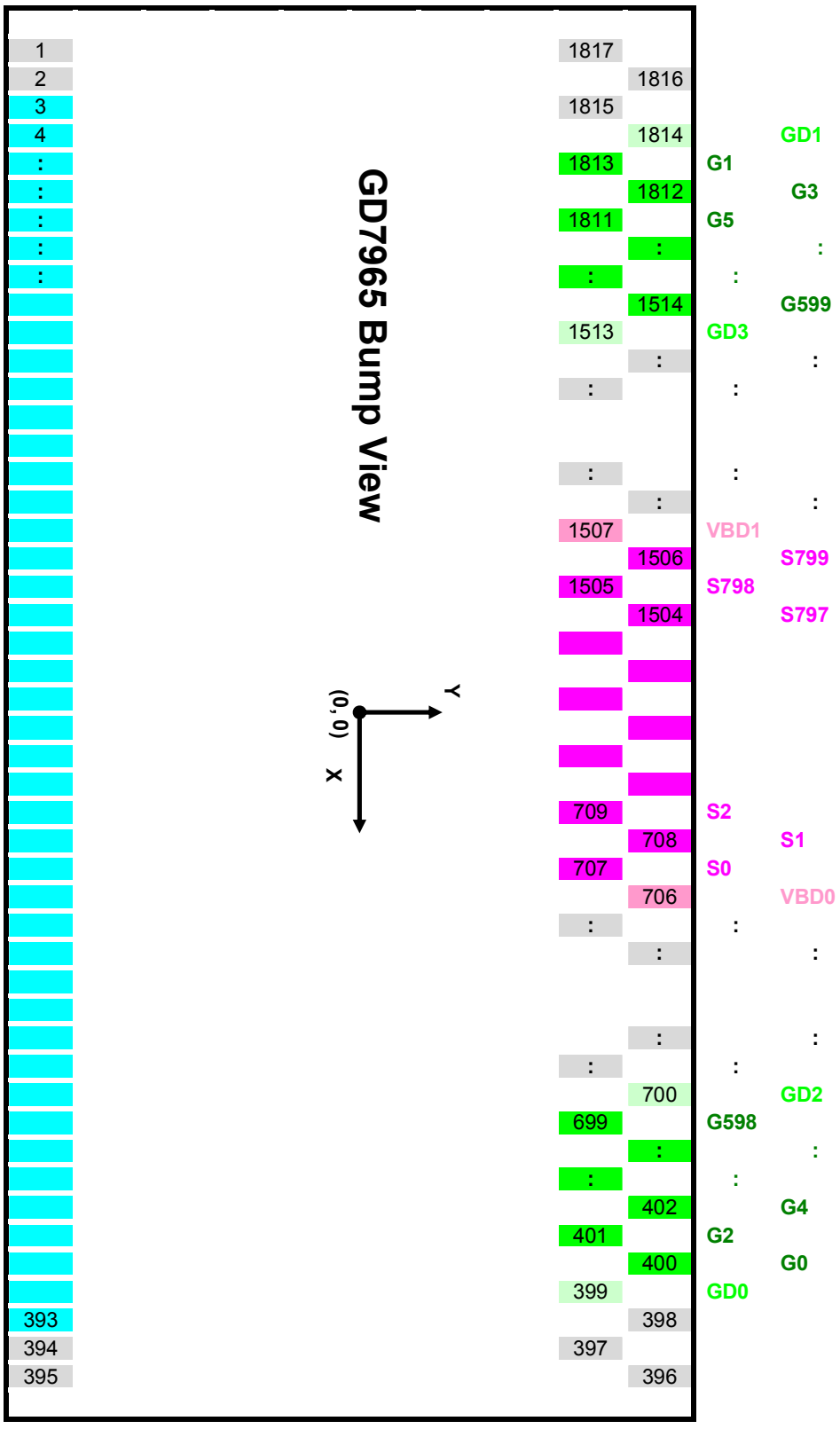

TRAY INFORMATION

(TBD)

REVISION HISTORY

Revision	Contents	Date
	(N/A)	