2.5 V to 5.5 V Octal Voltage Output 8-/10-/12-Bit DACs in 16-Lead TSSOP

AD5308/AD5318/AD5328

FEATURES

- AD5308: 8 buffered 8-bit DACs in 16-lead TSSOP
  - A version: ±1 LSB INL, B version: ±0.75 LSB INL
- AD5318: 8 buffered 10-bit DACs in 16-lead TSSOP
  - A version: ±4 LSB INL, B version: ±3 LSB INL
- AD5328: 8 buffered 12-bit DACs in 16-lead TSSOP
  - A version: ±16 LSB INL, B version: ±12 LSB INL
- Low power operation: 0.7 mA @ 3 V
- Guaranteed monotonic by design over all codes
- Power-down to 120 nA @ 3 V, 400 nA @ 5 V
- Double-buffered input logic
- Buffered/unbuffered/V_{DD} reference input options
- Output range: 0 V to V_{REF} or 0 V to 2 V_{REF}
- Power-on reset to 0 V
- Programmability
  - Individual channel power-down
  - Simultaneous update of outputs ($\overline{LDAC}$)
- Low power, SPI-®, QSPI-™, MICROWIRE-™, and DSP-compatible 3-wire serial interface
- On-chip rail-to-rail output buffer amplifiers
- Temperature range: −40°C to +105°C

APPLICATIONS

- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Optical networking
- Automatic test equipment
- Mobile communications
- Programmable attenuators
- Industrial process control

GENERAL DESCRIPTION

The AD5308/AD5318/AD5328 are octal 8-, 10-, and 12-bit buffered voltage output DACs in a 16-lead TSSOP. They operate from a single 2.5 V to 5.5 V supply, consuming 0.7 mA typical at 3 V. Their on-chip output amplifiers allow the outputs to swing rail-to-rail with a slew rate of 0.7 V/µs. The AD5308/AD5318/AD5328 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards.

The references for the eight DACs are derived from two reference pins (one per DAC quad). These reference inputs can be configured as buffered, unbuffered, or V_{DD} inputs. The parts incorporate a power-on reset circuit, which ensures that the DAC outputs power up to 0 V and remain there until a valid write to the device takes place. The outputs of all DACs may be updated simultaneously using the asynchronous $\overline{LDAC}$ input. The parts contain a power-down feature that reduces the current consumption of the devices to 400 nA at 5 V (120 nA at 3 V). The eight channels of the DAC may be powered down individually.

All three parts are offered in the same pinout, which allows users to select the resolution appropriate for their application without redesigning their circuit board.

Rev. D

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FUNCTIONAL BLOCK DIAGRAM

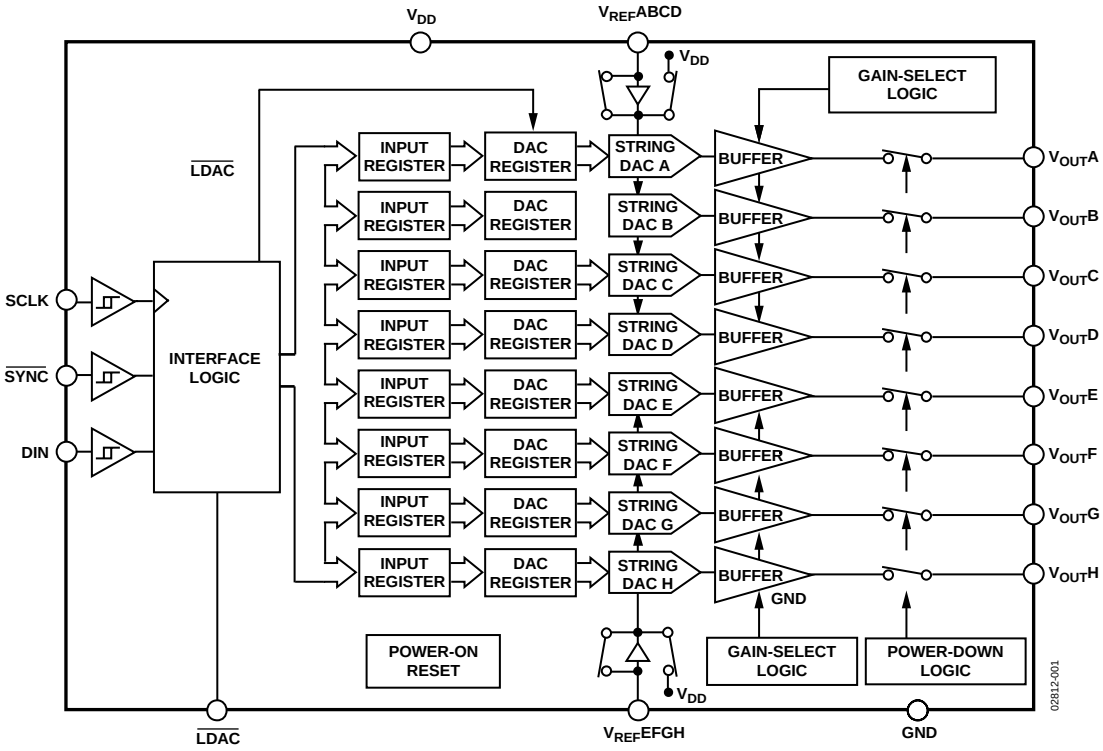


Figure 1.

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise specified.

Table 1.

	A Version[1]			B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[3, 4]								
AD5308								
Resolution	8			8			Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.75	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5318								
Resolution	10			10			Bits	
Relative Accuracy		±0.5	±4		±0.5	±3	LSB	
Differential Nonlinearity		±0.05	±0.50		±0.05	±0.50	LSB	Guaranteed monotonic by design over all codes
AD5328								
Resolution	12			12			Bits	
Relative Accuracy		±2	±16		±2	±12	LSB	
Differential Nonlinearity		±0.2	±1.0		±0.2	±1.0	LSB	Guaranteed monotonic by design over all codes
Offset Error		±5	±60		±5	±60	mV	V_{DD} = 4.5 V, gain = 2, see Figure 27 and Figure 28
Gain Error		±0.30	±1.25		±0.30	±1.25	% of FSR	V_{DD} = 4.5 V, gain = 2, see Figure 27 and Figure 28
Lower Deadband[5]		10	60		10	60	mV	Lower deadband exists only if offset error is negative, see Figure 27
Upper Deadband[5]		10	60		10	60	mV	Upper deadband exists only if $V_{REF} = V_{DD}$ and offset plus gain error is positive, see Figure 28
Offset Error Drift[6]		−12			−12		ppm of FSR/°C	
Gain Error Drift[6]		−5			−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		−60			−60		dB	V_{DD} = ±10%
DC Crosstalk[6]		200			200		µV	R_L = 2 kΩ to GND or V_{DD}
DAC REFERENCE INPUTS[6]								
V_{REF} Input Range	1.0		V_{DD}	1.0		V_{DD}	V	Buffered reference mode
	0.25		V_{DD}	0.25		V_{DD}	V	Unbuffered reference mode
V_{REF} Input Impedance (R_{DAC})		>10.0			>10.0		MΩ	Buffered reference mode and power-down mode
	37.0	45.0		37.0	45.0		kΩ	Unbuffered reference mode, 0 V to V_{REF} output range
	18.0	22.0		18.0	22.0		kΩ	Unbuffered reference mode, 0 V to 2 V_{REF} output range
Reference Feedthrough		−70.0			−70.0		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−75.0			−75.0		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]								
Minimum Output Voltage[7]		0.001			0.001		V	This is a measure of the minimum and maximum
Maximum Output Voltage[7]		V_{DD} − 0.001			V_{DD} − 0.001		V	Drive capability of the output amplifier
DC Output Impedance		0.5			0.5		Ω	

Parameter[2]	A Version[1] Min	A Version[1] Typ	A Version[1] Max	B Version[1] Min	B Version[1] Typ	B Version[1] Max	Unit	Conditions/Comments
Short Circuit Current		25.0			25.0		mA	V_{DD} = 5 V
		16.0			16.0		mA	V_{DD} = 3 V
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5.0			5.0		µs	Coming out of power-down mode, V_{DD} = 3 V
LOGIC INPUTS[6]								
Input Current			±1			±1	µA	
V_{IL}, Input Low Voltage			0.8			0.8	V	V_{DD} = 5 V ± 10%
			0.8			0.8	V	V_{DD} = 3 V ± 10%
			0.7			0.7	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	1.7			1.7			V	V_{DD} = 2.5 V to 5.5 V, TTL and CMOS compatible
Pin Capacitance		3.0			3.0		pF	
POWER REQUIREMENTS								
V_{DD}	2.5		5.5	2.5		5.5	V	
I_{DD} (Normal Mode)[8]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		1.0	1.8		1.0	1.8	mA	All DACs in unbuffered mode, in buffered mode
V_{DD} = 2.5 V to 3.6 V		0.7	1.5		0.7	1.5	mA	Extra current is typically x µA per DAC; x = (5 µA + V_{REF}/R_{DAC})/4
I_{DD} (Power-Down Mode)[9]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.4	1		0.4	1	µA	
V_{DD} = 2.5 V to 3.6 V		0.12	1		0.12	1	µA	

[1] Temperature range (A, B Version): −40°C to +105°C; typical at 25°C.
[2] See the Terminology section.
[3] DC specifications tested with the outputs unloaded unless stated otherwise.
[4] Linearity is tested using a reduced code range: AD5308 (Code 8 to Code 255), AD5318 (Code 28 to Code 1023), and AD5328 (Code 115 to Code 4095).
[5] This corresponds to x codes. x = deadband voltage/LSB size.
[6] Guaranteed by design and characterization; not production tested.
[7] For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and offset plus gain error must be positive.
[8] Interface inactive. All DACs active. DAC outputs unloaded.
[9] All eight DACs powered down.

V_{DD} = 2.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. AC Characteristics[1]

Parameter[3]	A, B Version[2] Min	A, B Version[2] Typ	A, B Version[2] Max	Unit	Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
AD5308		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0)
AD5318		7	9	µs	1/4 scale to 3/4 scale change (0x100 To 0x300)
AD5328		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.5		nV-sec	
Digital Crosstalk		0.5		nV-sec	
Analog Crosstalk		1		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p, unbuffered mode
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] Temperature range (A, B Version): –40°C to +105°C; typical at 25°C.
[3] See the Terminology section.

Table 3. Timing Characteristics[1, 2, 3]

Parameter	A, B Version Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ to SCLK falling edge set up time
t_5	5	ns min	Data set up time
t_6	4.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	50	ns min	Minimum $\overline{SYNC}$ high time
t_9	20	ns min	$\overline{LDAC}$ pulse width
t_{10}	20	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{11}	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] See Figure 2.

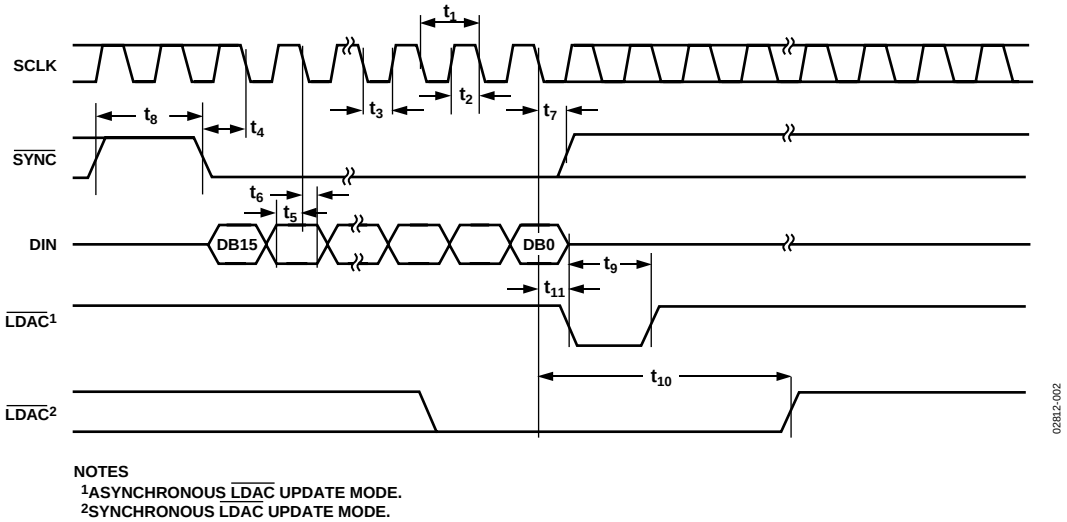


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Rating[1]
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUTA}–V_{OUTD} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A, B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	150°C
16-Lead TSSOP	
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature	JEDEC industry-standard
Soldering	J-STD-020

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

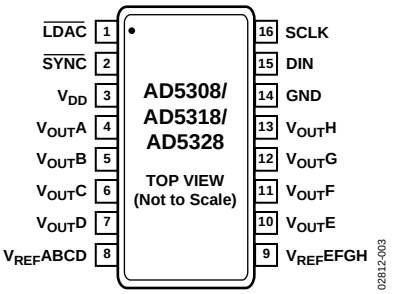


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	This active low control input transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous updates of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 16 clocks. If $\overline{\text{SYNC}}$ is taken high before the 16th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	$V_{OUT}C$	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
7	$V_{OUT}D$	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
8	$V_{REF}ABCD$	Reference Input Pin for DACs A, B, C, and D. It can be configured as a buffered, unbuffered, or V_{DD} input to the four DACs, depending on the state of the BUF and V_{DD} control bits. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
9	$V_{REF}EFGH$	Reference Input Pin for DACs E, F, G, and H. It can be configured as a buffered, unbuffered, or V_{DD} input to the four DACs, depending on the state of the BUF and V_{DD} control bits. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
10	$V_{OUT}E$	Buffered Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
11	$V_{OUT}F$	Buffered Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
12	$V_{OUT}G$	Buffered Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
13	$V_{OUT}H$	Buffered Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
14	GND	Ground Reference Point for All Circuitry on the Part.
15	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz. The SCLK input buffer is powered down after each write cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

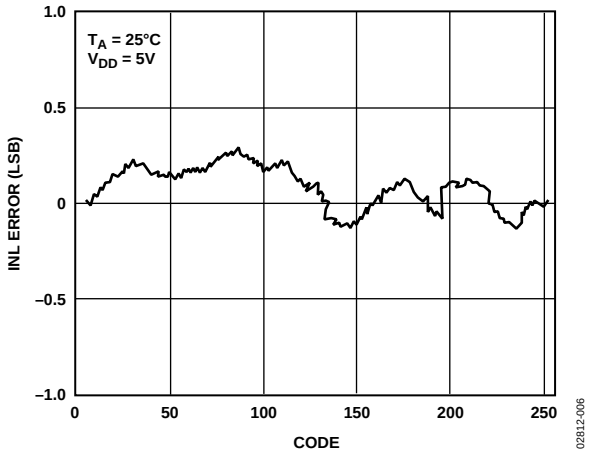


Figure 4. AD5308 Typical INL Plot

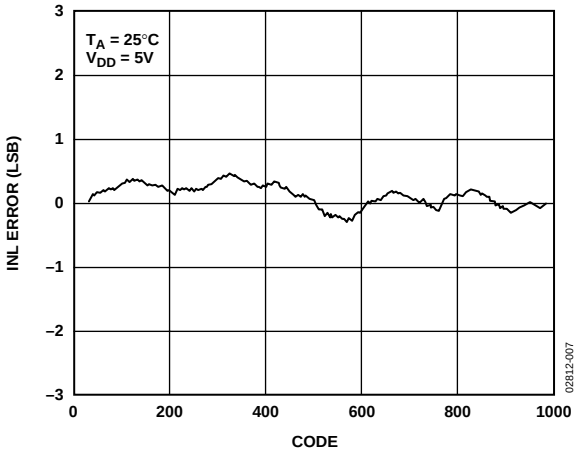


Figure 5. AD5318 Typical INL Plot

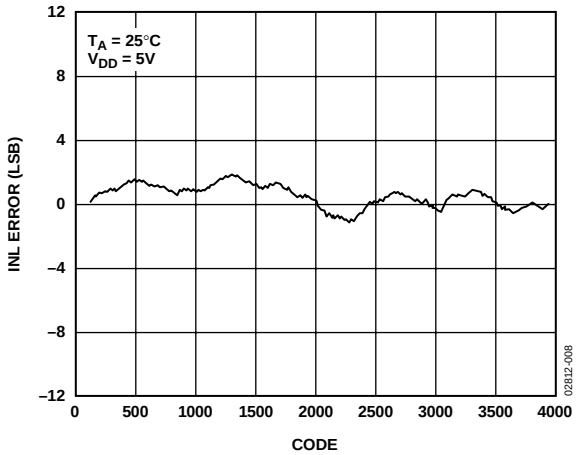


Figure 6. AD5328 Typical INL Plot

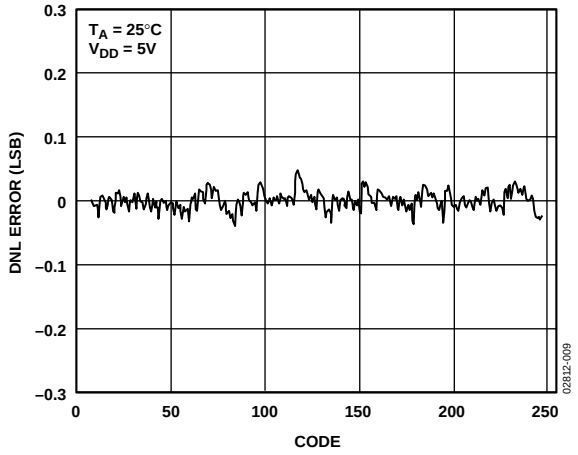


Figure 7. AD5308 Typical DNL Plot

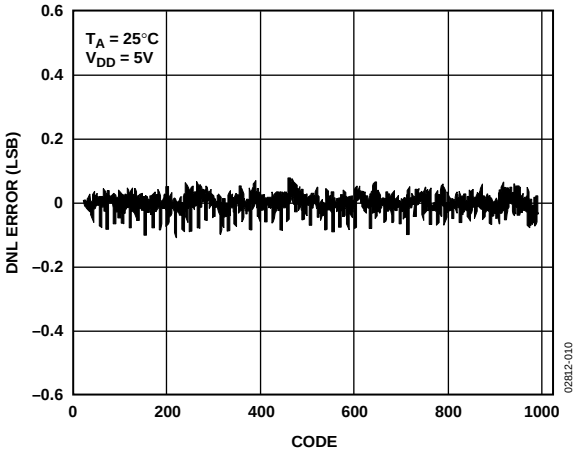


Figure 8. AD5318 Typical DNL Plot

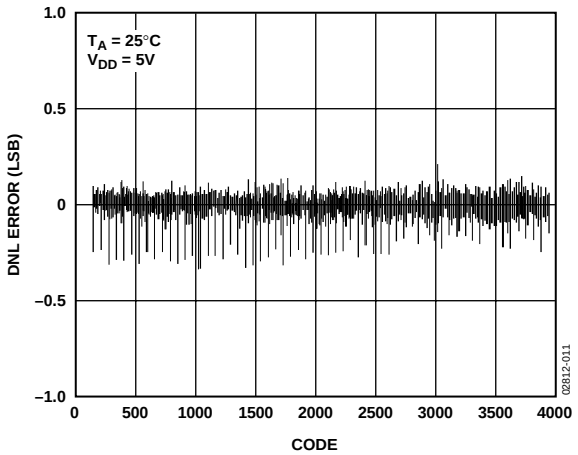


Figure 9. AD5328 Typical DNL Plot

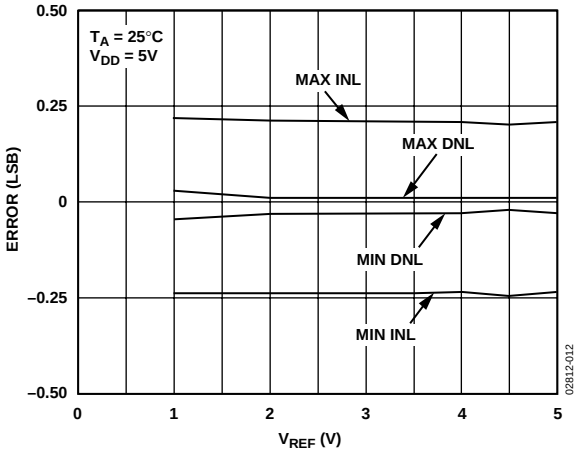


Figure 10. AD5308 INL and DNL Error vs. V_{REF}

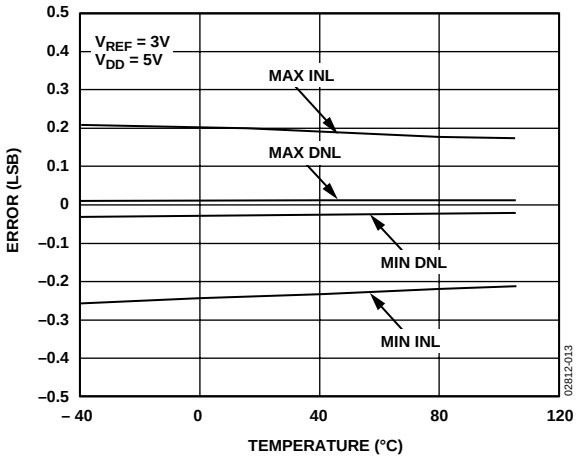


Figure 11. AD5308 INL Error and DNL Error vs. Temperature

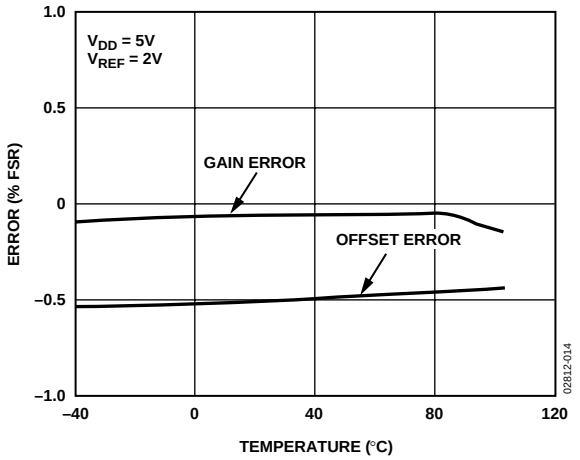


Figure 12. AD5308 Offset Error and Gain Error vs. Temperature

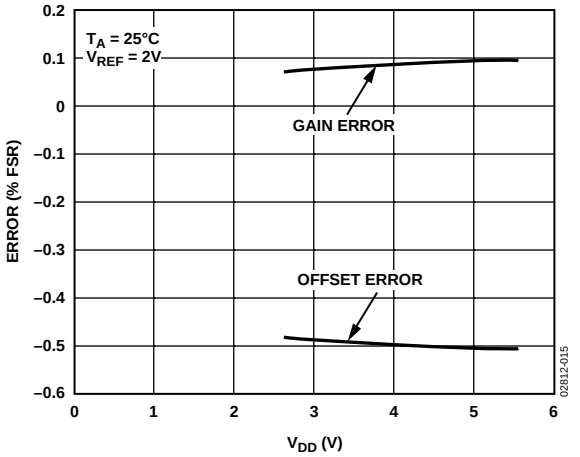


Figure 13. Offset Error and Gain Error vs. V_{DD}

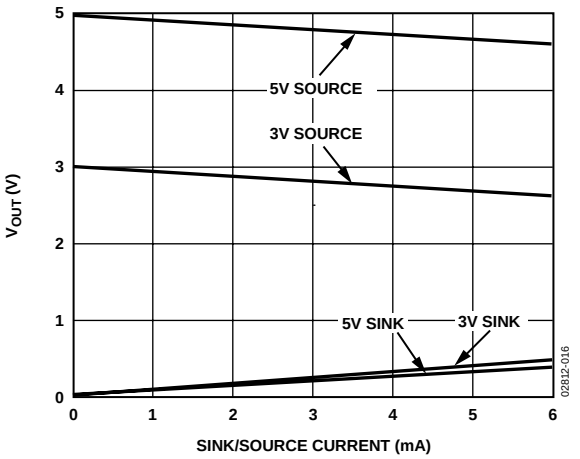


Figure 14. V_{OUT} Source and Sink Current Capability

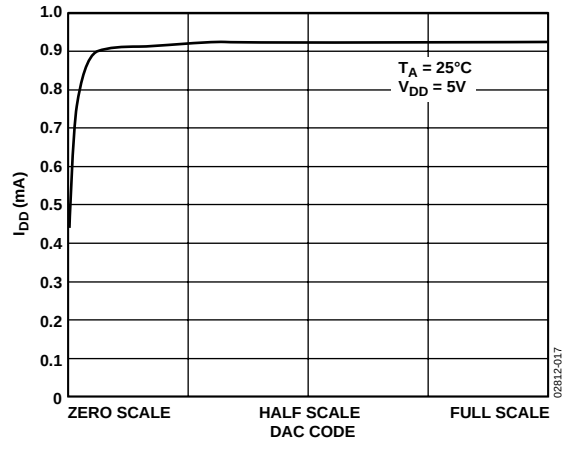


Figure 15. Supply Current vs. DAC Code

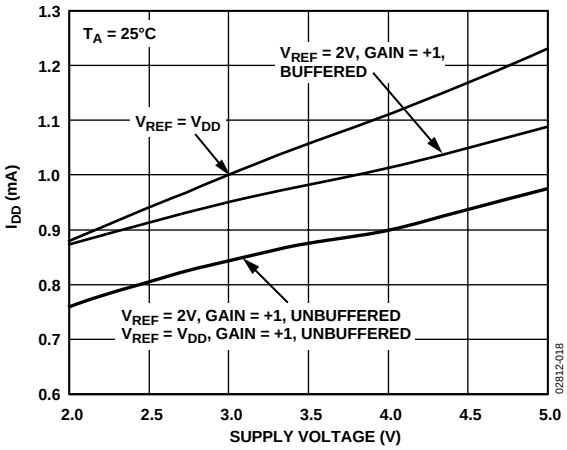


Figure 16. Supply Current vs. Supply Voltage

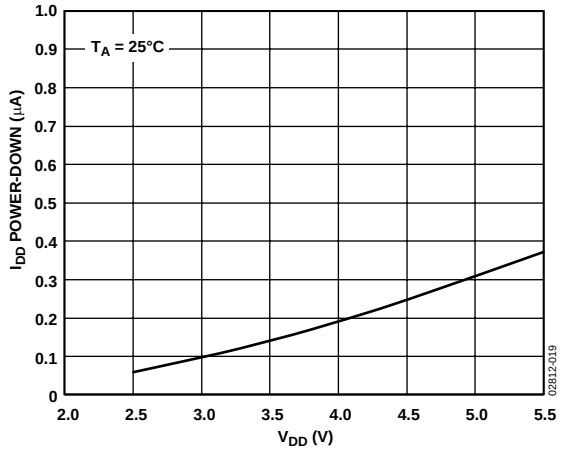


Figure 17. Power-Down Current vs. Supply Voltage

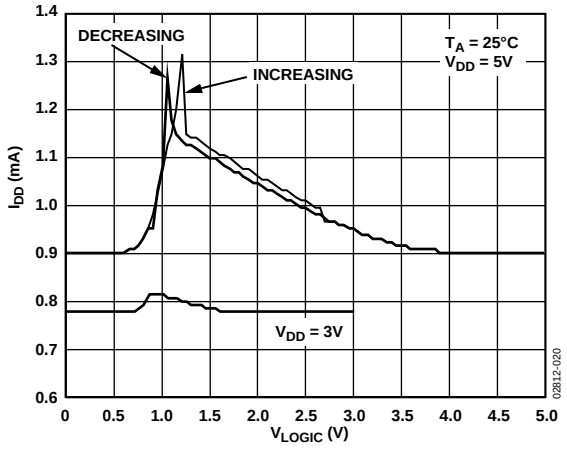


Figure 18. Supply Current vs. Logic Input Voltage for SCLK and DIN Increasing and Decreasing

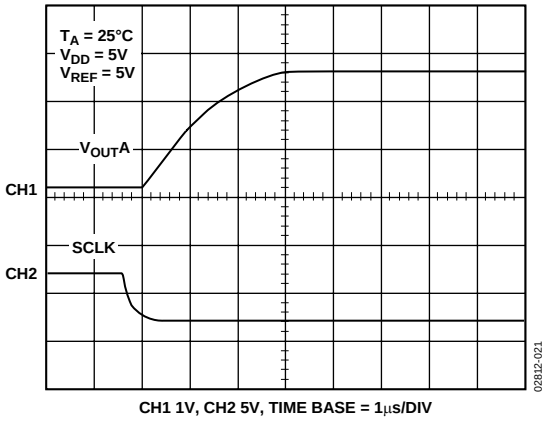


Figure 19. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

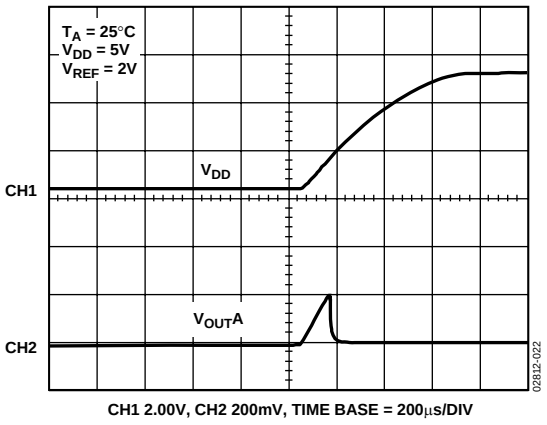


Figure 20. Power-On Reset to 0 V

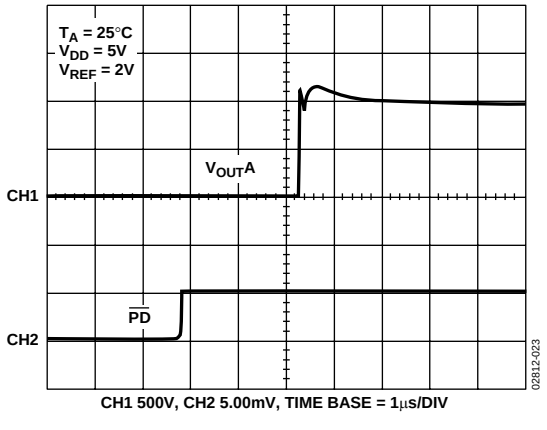


Figure 21. Exiting Power-Down to Midscale

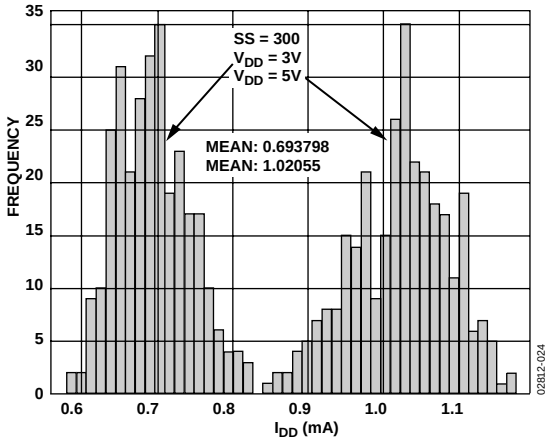


Figure 22. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

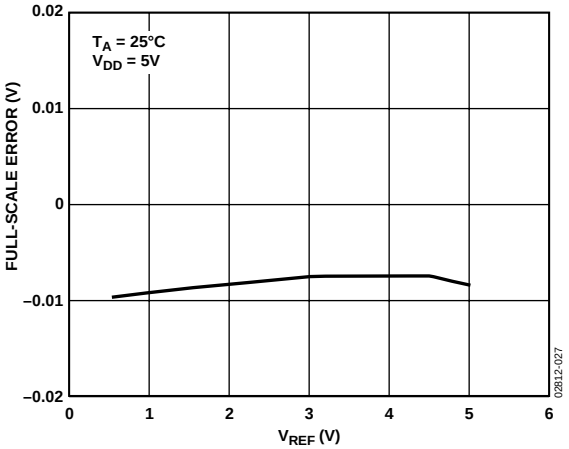


Figure 25. Full-Scale Error vs. V_{REF}

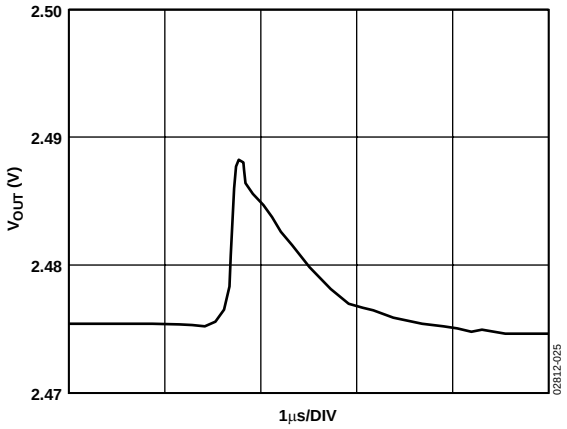


Figure 23. AD5328 Major-Code Transition Glitch Energy

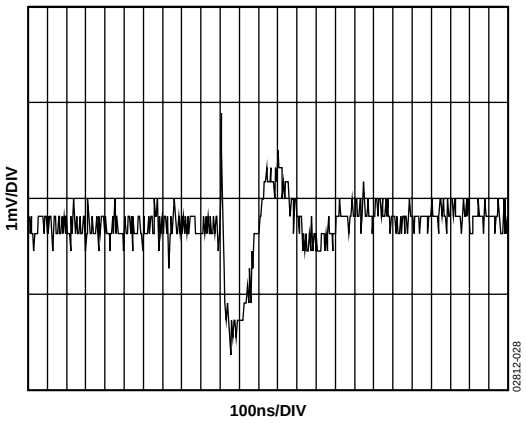


Figure 26. DAC-to-DAC Crosstalk

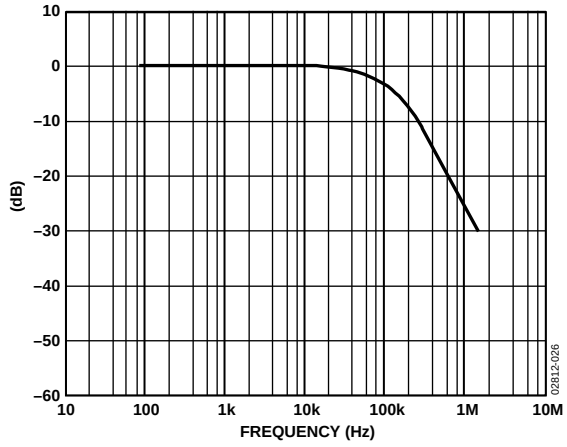


Figure 24. Multiplying Bandwidth (Small-Signal Frequency Response)

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. Typical INL vs. code plots can be seen in Figure 4, Figure 5, and Figure 6.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. code plots can be seen in Figure 7, Figure 8, and Figure 9.

Offset Error
This is a measure of the offset error of the DAC and the output amplifier (see Figure 27 and Figure 28). It can be negative or positive, and is expressed in millivolts.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift
This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk
This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in microvolts.

Reference Feedthrough
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Channel-to-Channel Isolation
This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in decibels.

Major-Code Transition Glitch Energy
Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital code is changed by 1 LSB at the major carry transition (011 ... 11 to 100 ... 00 or 100 ... 00 to 011 ... 11).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-sec and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s and vice versa.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code is not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

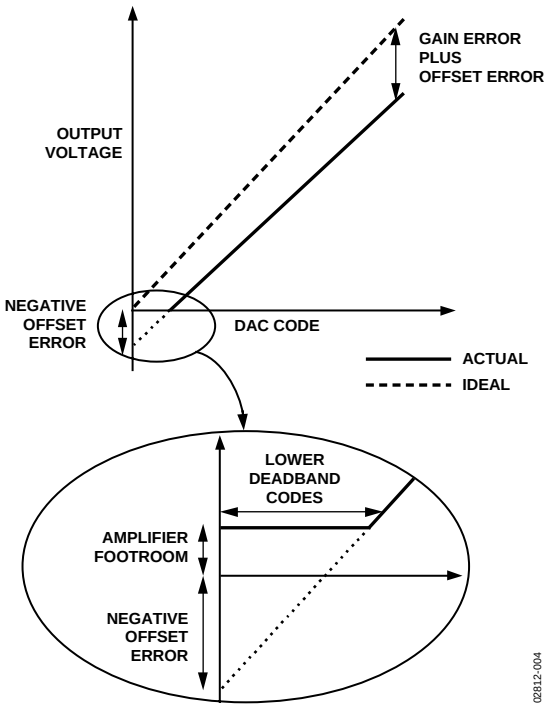


Figure 27. Transfer Function with Negative Offset ($V_{REF} = V_{DD}$)

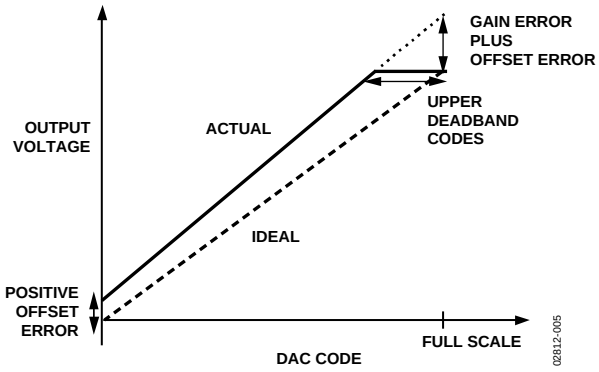


Figure 28. Transfer Function with Positive Offset

THEORY OF OPERATION

The AD5308/AD5318/AD5328 are octal resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. Each contains eight output buffer amplifiers and is written to via a 3-wire serial interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. DAC A, DAC B, DAC C, and DAC D share a common reference input, V_{REF}ABCD. DAC E, DAC F, DAC G, and DAC H share a common reference input, V_{REF}EFGH. Each reference input can be buffered to draw virtually no current from the reference source, can be unbuffered to give a reference input range from 0.25 V to V_{DD}, or can come from V_{DD}. The devices have a power-down mode in which all DACs can be turned off individually with a high impedance output.

DIGITAL-TO-ANALOG CONVERTER

The architecture of one DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the corresponding DAC. Figure 29 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register:
0 to 255 for AD5308 (8 bits)
0 to 1023 for AD5318 (10 bits)
0 to 4095 for AD5328 (12 bits)
N is the DAC resolution.

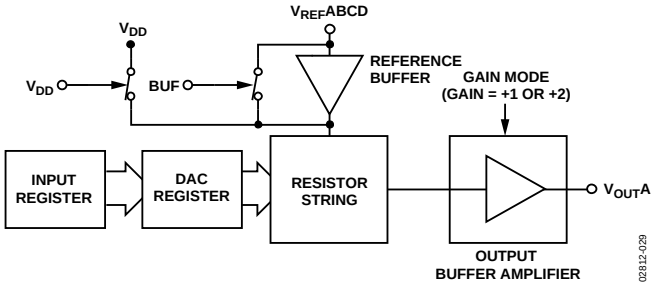


Figure 29. Single DAC Channel Architecture

DAC Reference Inputs

There is a reference pin for each quad of DACs. The reference inputs can be buffered from V_{DD}, or unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However, if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V_{DD} since there is no restriction due to the headroom and footroom of the reference amplifier.

If there is a buffered reference in the circuit (for example, the REF192), there is no need to use the on-chip buffers of the AD5308/AD5318/AD5328. In unbuffered mode, the input impedance is still large at typically 45 kΩ per reference input for 0 V to V_{REF} mode and 22 kΩ for 0 V to 2 V_{REF} mode.

RESISTOR STRING

The resistor-string section is shown in Figure 30. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

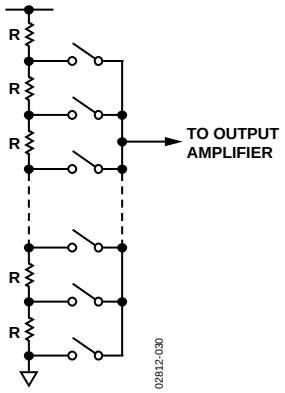


Figure 30. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, the gain of the output amplifier, the offset error, and the gain error.

If a gain of 1 is selected (gain bit = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (gain bit = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to V_{DD} − 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in the plot in Figure 14.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 µs.

POWER-ON RESET

The AD5308/AD5318/AD5328 are provided with a power-on reset function so that they power up in a defined state. The power-on state is

- Normal operation
- Reference inputs unbuffered
- 0 V to V_{REF} output range
- Output voltage set to 0 V
- $\overline{\text{LDAC}}$ bits set to $\overline{\text{LDAC}}$ high

Both input and DAC registers are filled with 0s and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

POWER-DOWN MODE

The AD5308/AD5318/AD5328 have low power consumption, typically dissipating 2.4 mW with a 3 V supply and 5 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is described in the Serial Interface section.

When in default mode, all DACs work normally with a typical power consumption of 1 mA at 5 V (800 μA at 3 V). However, when all DACs are powered down, that is, in power-down mode, the supply current falls to 400 nA at 5 V (120 nA at 3 V). Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the output is three-state while the part is in power-down mode, and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure 31.

The bias generator, the output amplifiers, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. In fact, it is possible to load new data to the input registers and DAC registers during power-down. The DAC outputs update as soon as the device comes out of power-down mode. The time to exit power-down is typically 2.5 μs when V_{DD} = 5 V and 5 μs when V_{DD} = 3 V.

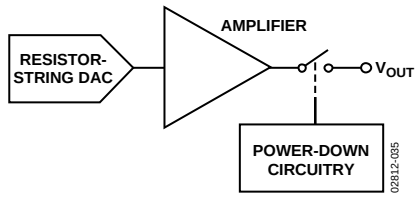


Figure 31. Output Stage During Power-Down

SERIAL INTERFACE

The AD5308/AD5318/AD5328 are controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 2.

The $\overline{\text{SYNC}}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low, observing the minimum $\overline{\text{SYNC}}$ to SCLK falling edge set-up time, t_4. After $\overline{\text{SYNC}}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses.

To end the transfer, $\overline{\text{SYNC}}$ must be taken high after the falling edge of the 16th SCLK pulse, observing the minimum SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time, t_7.

After the end of the serial data transfer, data is automatically transferred from the input shift register to the input register of the selected DAC. If $\overline{\text{SYNC}}$ is taken high before the 16th falling edge of SCLK, the data transfer is aborted and the DAC input registers are not updated.

Data is loaded MSB first (Bit 15). The first bit determines whether it is a DAC write or a control function.

DAC Write

The 16-bit word consists of 1 control bit and 3 address bits followed by 8, 10, or 12 bits of DAC data, depending on the device type. In the case of a DAC write, the MSB is a 0. The next 3 address bits determine whether the data is for DAC A, DAC B, DAC C, DAC D, DAC E, DAC F, DAC G, or DAC H. The AD5328 uses all 12 bits of DAC data. The AD5318 uses 10 bits and ignores the 2 LSBs. The AD5308 uses 8 bits and ignores the last 4 bits. These ignored LSBs should be set to 0. The data format is straight binary, with all 0s corresponding to 0 V output and all 1s corresponding to full-scale output.

Table 6. Address Bits for the AD5308/AD5318/AD5328

A2 (Bit 14)	A1 (Bit 13)	A0 (Bit 12)	DAC Addressed
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	0	0	DAC E
1	0	1	DAC F
1	1	0	DAC G
1	1	1	DAC H

Control Functions

In the case of a control function, the MSB (Bit 15) is a 1. This is followed by two control bits, which determine the mode. There are four different control modes: reference and gain mode, $\overline{\text{LDAC}}$ mode, power-down mode, and reset mode. The write sequences for these modes are shown in Table 7.

Reference and Gain Mode

This mode determines whether the reference for each group of DACs is buffered, unbuffered, or from V_{DD}. It also determines the gain of the output amplifier. To set up the reference of both groups, set the control bits to (00), set the GAIN bits, the BUF bits, and the V_{DD} bits.

BUF

This controls whether the reference of a group of DACs is buffered or unbuffered. The reference of the first group of DACs (A, B, C, and D) is controlled by setting Bit 2, and the second group of DACs (E, F, G, and H) is controlled by setting Bit 3.

0: unbuffered reference.
1: buffered reference.

GAIN

The gain of the DACs is controlled by setting Bit 4 for the first group of DACs (A, B, C, and D) and Bit 5 for the second group of DACs (E, F, G, and H).

0: output range of 0 V to V_{REF}.
1: output range of 0 V to 2 V_{REF}.

Table 7. Control Words for the AD53x8

$\overline{\text{D}}$/C	Control Bits															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Mode
										GAIN Bits		BUF Bits		V_{DD} Bits		Gain of output amplifier and
1	0	0	x	x	x	x	x	x	x	E...H	A...D	E...H	A...D	E...H	A...D	reference selection
														$\overline{\text{LDAC}}$ Bits		
1	0	1	x	x	x	x	x	x	x	x		x	x	1/0	1/0	$\overline{\text{LDAC}}$
														Channels		
1	1	0	x	x	x	x	x	H	G	F	E	D	C	B	A	Power-down
		Reset														
1	1	1	1/0	x	x	x	x	x	x	x	x	x	x	x	x	Reset

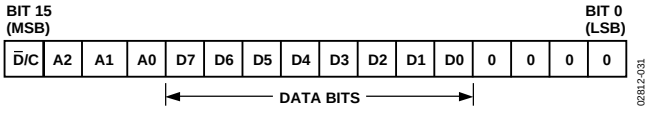


Figure 32. AD5308 Input Shift Register Contents

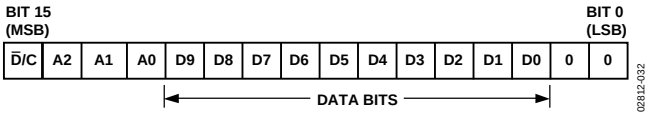


Figure 33. AD5318 Input Shift Register Contents

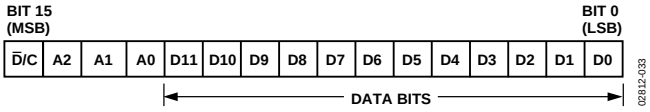


Figure 34. AD5328 Input Shift Register Contents

V_{DD}

These bits are set when V_{DD} is to be used as a reference. The first group of DACs (A, B, C, and D) can be set up to use V_{DD} by setting Bit 0, and the second group of DACs (E, F, G, and H) by setting Bit 1. The V_{DD} bits have priority over the BUF bits.

When V_{DD} is used as the reference, it is always unbuffered and has an output range of 0 V to V_{REF} regardless of the state of the GAIN and BUF bits.

$\overline{\text{LDAC}}$ Mode

$\overline{\text{LDAC}}$ mode controls $\overline{\text{LDAC}}$, which determines when data is transferred from the input registers to the DAC registers. There are three options when updating the DAC registers, as shown in Table 8.

Table 8. $\overline{\text{LDAC}}$ Mode

Bit 15	Bit 14	Bit 13	Bits 12:2	Bit 1	Bit 0	Description
1	0	1	x ... x	0	0	$\overline{\text{LDAC}}$ low
1	0	1	x ... x	0	1	$\overline{\text{LDAC}}$ high
1	0	1	x ... x	1	0	$\overline{\text{LDAC}}$ single update
1	0	1	x ... x	1	1	Reserved

$\overline{\text{LDAC}}$ Low (00): This option sets $\overline{\text{LDAC}}$ permanently low, allowing the DAC registers to be updated continuously.

$\overline{\text{LDAC}}$ High (01): This option sets $\overline{\text{LDAC}}$ permanently high. The DAC registers are latched and the input registers can change without affecting the contents of the DAC registers. This is the default option for this mode.

$\overline{\text{LDAC}}$ Single Update (10): This option causes a single pulse on $\overline{\text{LDAC}}$, updating the DAC registers once.

Reserved (11): reserved.

Power-Down Mode

The individual channels of the AD5308/AD5318/AD5328 can be powered down separately. The control mode for this is (10). On completion of this write sequence, the channels that have been set to 1 are powered down.

Reset Mode

This mode consists of two possible reset functions, as outlined in Table 9.

Table 9. Reset Mode

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 ... 0	Description
1	1	1	0	x ... x	DAC data reset
1	1	1	1	x ... x	Data and control reset

DAC Data Reset: On completion of this write sequence, all DAC registers and input registers are filled with 0s.

Data and Control Reset: This function carries out a DAC data reset and resets all the control bits (GAIN, BUF, V_{DD}, $\overline{\text{LDAC}}$, and power-down channels) to their power-on conditions.

LOW POWER SERIAL INTERFACE

To minimize the power consumption of the device, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$. The SCLK and DIN input buffers are powered down on the rising edge of $\overline{\text{SYNC}}$.

LOAD DAC INPUT ($\overline{\text{LDAC}}$) FUNCTION

Access to the DAC registers is controlled by both the $\overline{\text{LDAC}}$ pin and the $\overline{\text{LDAC}}$ mode bits. The operation of the $\overline{\text{LDAC}}$ function can be likened to the configuration shown in Figure 35.

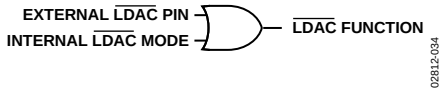


Figure 35. $\overline{\text{LDAC}}$ Function

If the user wishes to update the DAC through software, the $\overline{\text{LDAC}}$ pin should be tied high and the $\overline{\text{LDAC}}$ mode bits set as required. Alternatively, if the user wishes to control the DAC through hardware, that is, the $\overline{\text{LDAC}}$ pin, the $\overline{\text{LDAC}}$ mode bits should be set to $\overline{\text{LDAC}}$ high (default mode).

Use of the $\overline{\text{LDAC}}$ function enables double-buffering of the DAC data, and the GAIN, BUF and V_{DD} bits. There are two ways in which the $\overline{\text{LDAC}}$ function can operate:

Synchronous $\overline{\text{LDAC}}$: The DAC registers are updated after new data is read in on the falling edge of the 16th SCLK pulse. $\overline{\text{LDAC}}$ can be permanently low or pulsed as in Figure 2.

Asynchronous $\overline{\text{LDAC}}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

DOUBLE-BUFFERED INTERFACE

The AD5308/AD5318/AD5328 DACs all have double-buffered interfaces consisting of two banks of registers: input and DAC. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

When the $\overline{\text{LDAC}}$ pin is high and the $\overline{\text{LDAC}}$ bits are set to (01), the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. However, when the $\overline{\text{LDAC}}$ bits are set to (00) or when the $\overline{\text{LDAC}}$ pin is brought low, the DAC registers become transparent and the contents of the input registers are transferred to them.

The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write up to seven of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the remaining DAC input register, all outputs will update simultaneously.

These parts contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5308/AD5318/AD5328, the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

MICROPROCESSOR INTERFACE

ADSP-2101/ADSP-2103-to-AD5308/AD5318/AD5328 INTERFACE

Figure 36 shows a serial interface between the AD5308/AD5318/ AD5328 and the ADSP-2101/ADSP-2103. The ADSP-2101/ ADSP-2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. The data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5308/AD5318/ AD5328 on the falling edge of the DAC's SCLK.

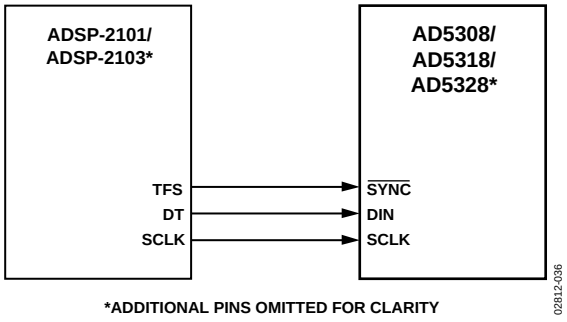


Figure 36. ADSP-2101/ADSP-2103-to-AD5308/AD5318/AD5328 Interface

68HC11/68L11-to-AD5308/AD5318/AD5328 INTERFACE

Figure 37 shows a serial interface between the AD5308/AD5318/ AD5328 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5308/AD5318/AD5328, and the MOSI output drives the serial data line (DIN) of the DAC. The sync signal is derived from a port line (PC7). The set up conditions for the correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the sync line is taken low (PC7). When the 68HC11/ 68L11 is configured as just described, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/ 68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5308/AD5318/AD5328, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

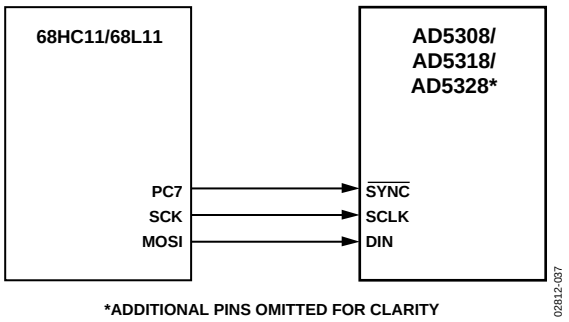


Figure 37. 68HC11/68L11-to-AD5308/AD5318/ AD5328 Interface

80C51/80L51-to-AD5308/AD5318/AD5328 INTERFACE

Figure 38 shows a serial interface between the AD5308/AD5318/ AD5328 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5308/AD5318/AD5328, while RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is transmitted to the AD5308/AD5318/AD5328, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5308/AD5318/AD5328 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

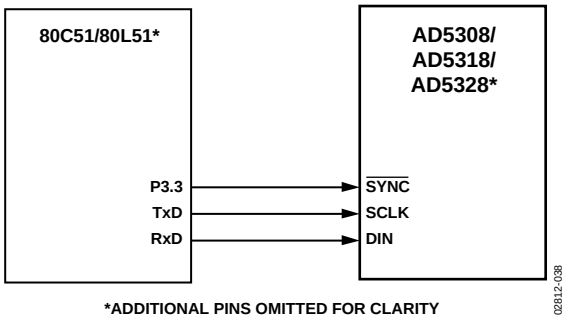


Figure 38. 80C51/80L51-to-AD5308/AD5318/AD5328 Interface

MICROWIRE-to-AD5308/AD5318/AD5328 INTERFACE

Figure 39 shows an interface between the AD5308/AD5318/AD5328 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the AD5308/AD5318/AD5328 on the rising edge of SK, which corresponds to the falling edge of the DAC's SCLK.

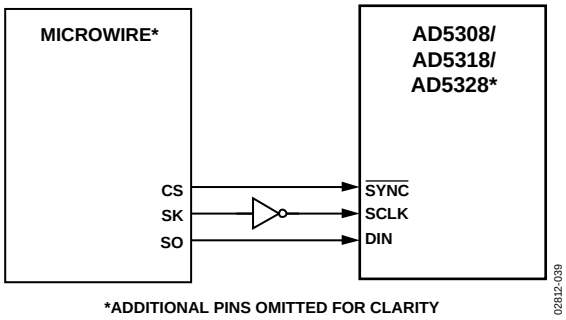


Figure 39. MICROWIRE-to-AD5308/AD5318/AD5328 Interface

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

The AD5308/AD5318/AD5328 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices are used with a fixed, precision reference voltage. Suitable references for 5 V operation are the AD780, ADR381, and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference is the AD589 or the AD1580 (1.2 V band gap references). Figure 40 shows a typical setup for the AD5308/AD5318/AD5328 when using an external reference.

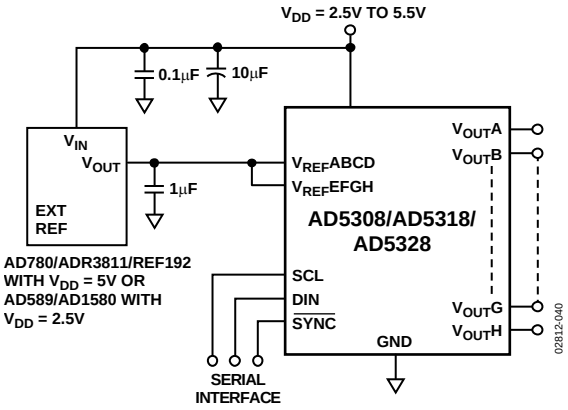


Figure 40. AD5308/AD5318/AD5328 Using a 2.5 V or 5 V External Reference

DRIVING V_{DD} FROM THE REFERENCE VOLTAGE

If an output range of 0 V to V_{DD} is required when the reference inputs are configured as unbuffered, the simplest solution is to connect the reference input to V_{DD}. As this supply can be noisy and not very accurate, the AD5308/AD5318/AD5328 can be powered from a voltage reference. For example, using a 5 V reference, such as the REF195, works because the REF195 outputs a steady supply voltage for the AD5308/AD5318/AD5328. The typical current required from the REF195 is a 1 µA supply current and ≈ 112 µA into the reference inputs (if unbuffered); this is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a10 kΩ load on each output) is

1.22 mA + 8(5 V/10 kΩ) = 5.22 mA

The load regulation of the REF195 is typically 2.0 ppm/mA, which results in an error of 10.4 ppm (52 µV) for the 5.22 mA current drawn from it. This corresponds to a 0.003 LSB error at 8 bits and 0.043 LSB error at 12 bits.

BIPOLAR OPERATION USING THE AD5308/AD5318/AD5328

The AD5308/AD5318/AD5328 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 41. This circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820, the AD8519, or an OP196 as the output amplifier.

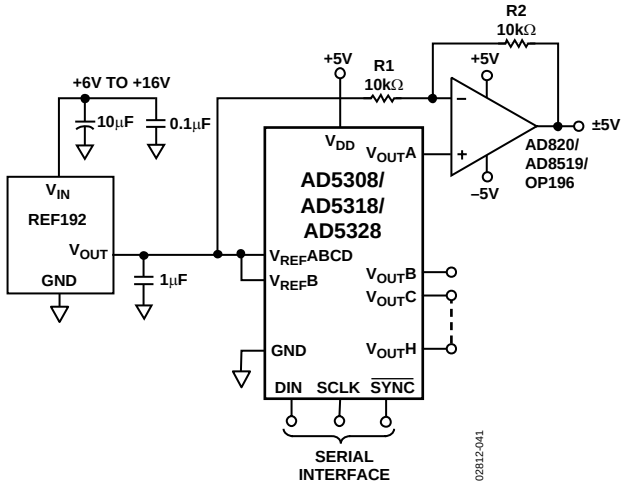


Figure 41. Bipolar Operation with the AD5308/AD5318/AD5328

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = \left[\frac{(REFIN \times D/2^N) \times (R1 + R2)}{R1}\right] - REFIN \times (R2/R1)$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
REFIN is the reference voltage input.

with

REFIN = 5 V , R1 = R2 = 10 kΩ

$$V_{OUT} = (10 \times D/2^N) - 5\ V$$

OPTO-ISOLATED INTERFACE FOR PROCESS CONTROL APPLICATIONS

The AD5308/AD5318/AD5328 have a versatile 3-wire serial interface, making them ideal for generating accurate voltages in process control and industrial applications. Due to noise and safety requirements, or distance, it may be necessary to isolate the AD5308/AD5318/AD5328 from the controller. This can easily be achieved by using opto-isolators that provide isolation in excess of 3 kV. The actual data rate achieved may be limited by the type of optocouplers chosen. The serial loading structure of the AD5308/AD5318/AD5328 makes them ideally suited for use in opto-isolated applications. Figure 42 shows an opto-isolated interface to the AD5308/AD5318/AD5328 where DIN, SCLK, and $\overline{\text{SYNC}}$ are driven from optocouplers. The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5308/AD5318/AD5328.

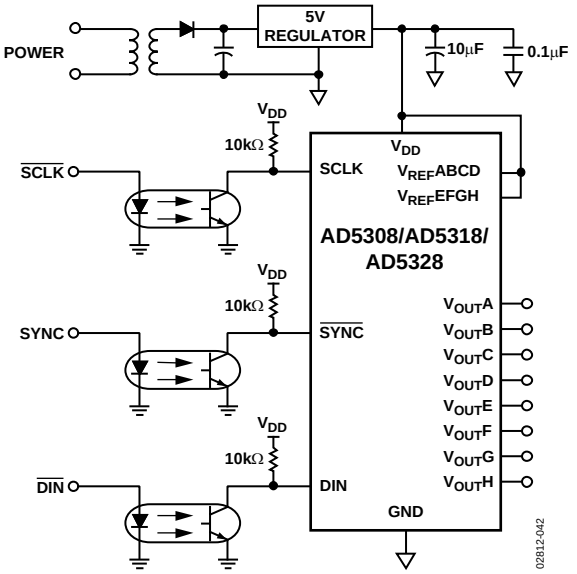


Figure 42. AD5308/AD5318/AD5328 in an Opto-Isolated Interface

DECODING MULTIPLE AD5308/AD5318/AD5328s

The $\overline{\text{SYNC}}$ pin on the AD5308/AD5318/AD5328 can be used in applications to decode a number of DACs. In this application, the DACs in the system receive the same serial clock and serial data but only the $\overline{\text{SYNC}}$ to one of the devices is active at any one time, allowing access to four channels in this 16-channel system. The 74HC139 is used as a 2-to-4 line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded-address inputs are changing state. Figure 43 shows a diagram of a typical setup for decoding multiple AD5308 devices in a system.

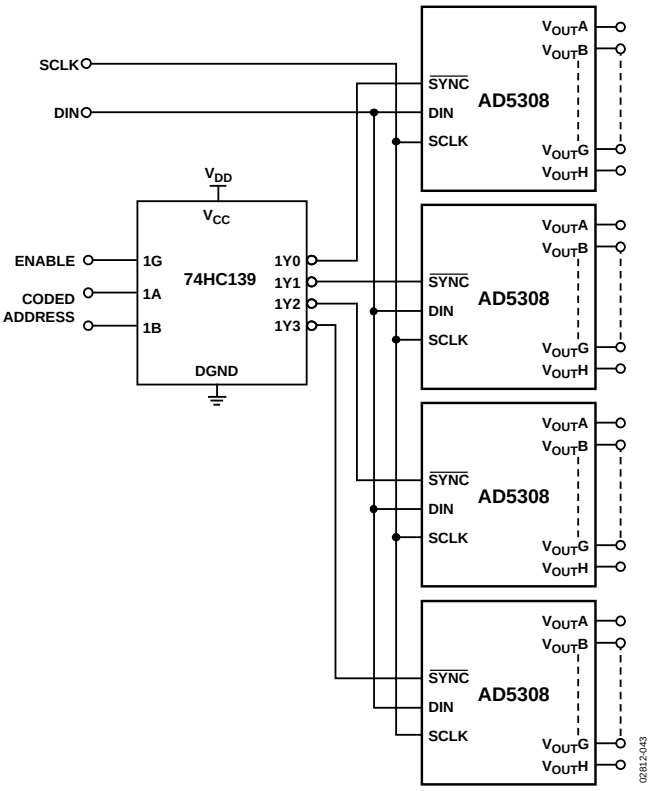


Figure 43. Decoding Multiple AD5308 Devices in a System

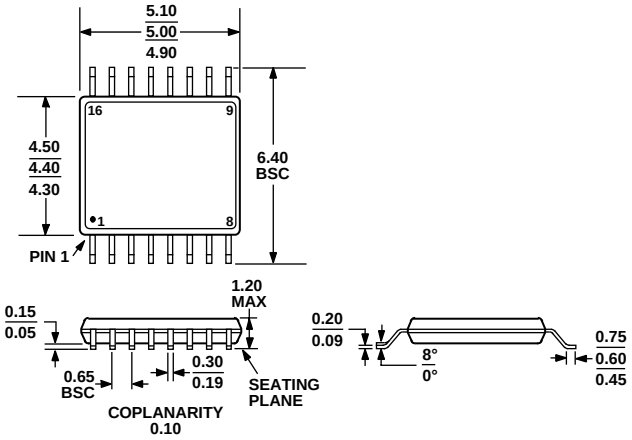
Table 10. Overview of AD53xx Serial Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time (µs)	Interface	Package	Pins
SINGLES							
AD5300	8	±0.25	0 ($V_{REF} = V_{DD}$)	4	SPI	SOT-23, MSOP	6, 8
AD5310	10	±0.50	0 ($V_{REF} = V_{DD}$)	6	SPI	SOT-23, MSOP	6, 8
AD5320	12	±1.00	0 ($V_{REF} = V_{DD}$)	8	SPI	SOT-23, MSOP	6, 8
AD5301	8	±0.25	0 ($V_{REF} = V_{DD}$)	6	2-Wire	SOT-23, MSOP	6, 8
AD5311	10	±0.50	0 ($V_{REF} = V_{DD}$)	7	2-Wire	SOT-23, MSOP	6, 8
AD5321	12	±1.00	0 ($V_{REF} = V_{DD}$)	8	2-Wire	SOT-23, MSOP	6, 8
DUALS							
AD5302	8	±0.25	2	6	SPI	MSOP	10
AD5312	10	±0.50	2	7	SPI	MSOP	10
AD5322	12	±1.00	2	8	SPI	MSOP	10
AD5303	8	±0.25	2	6	SPI	TSSOP	16
AD5313	10	±0.50	2	7	SPI	TSSOP	16
AD5323	12	±1.00	2	8	SPI	TSSOP	16
QUADS							
AD5304	8	±0.25	1	6	SPI	MSOP	10
AD5314	10	±0.50	1	7	SPI	MSOP	10
AD5324	12	±1.00	1	8	SPI	MSOP	10
AD5305	8	±0.25	1	6	2-Wire	MSOP	10
AD5315	10	±0.50	1	7	2-Wire	MSOP	10
AD5325	12	±1.00	1	8	2-Wire	MSOP	10
AD5306	8	±0.25	4	6	2-Wire	TSSOP	16
AD5316	10	±0.50	4	7	2-Wire	TSSOP	16
AD5326	12	±1.00	4	8	2-Wire	TSSOP	16
AD5307	8	±0.25	2	6	SPI	TSSOP	16
AD5317	10	±0.50	2	7	SPI	TSSOP	16
AD5327	12	±1.00	2	8	SPI	TSSOP	16
OCTALS							
AD5308	8	±0.25	2	6	SPI	TSSOP	16
AD5318	10	±0.50	2	7	SPI	TSSOP	16
AD5328	12	±1.00	2	8	SPI	TSSOP	16

Table 11. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time (µs)	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6	✓	✓		✓	TSSOP	20
AD5331	10	±0.50	1	7		✓		✓	TSSOP	20
AD5340	12	±1.00	1	8	✓	✓		✓	TSSOP	24
AD5341	12	±1.00	1	8	✓	✓	✓	✓	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6				✓	TSSOP	20
AD5333	10	±0.50	2	7	✓	✓		✓	TSSOP	24
AD5342	12	±1.00	2	8	✓	✓		✓	TSSOP	28
AD5343	12	±1.00	1	8			✓	✓	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6		✓		✓	TSSOP	24
AD5335	10	±0.50	2	7			✓	✓	TSSOP	24
AD5336	10	±0.50	4	7		✓		✓	TSSOP	28
AD5344	12	±1.00	4	8					TSSOP	28

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 44. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5308ARU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308ARU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308ARUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308ARUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRU-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRUZ-REEL[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5308BRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318ARU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318ARU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318ARUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318ARUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRU-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRUZ-REEL[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5318BRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328ARU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328ARU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328ARUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328ARUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRU	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRU-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRU-REEL7	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRUZ-REEL[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD5328BRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16

[1] Z = RoHS Compliant Part.

D02812-0-3/07(D)