DS28E01-100
1Kb Protected 1-Wire EEPROM with SHA-1 Engine

www.maxim-ic.com

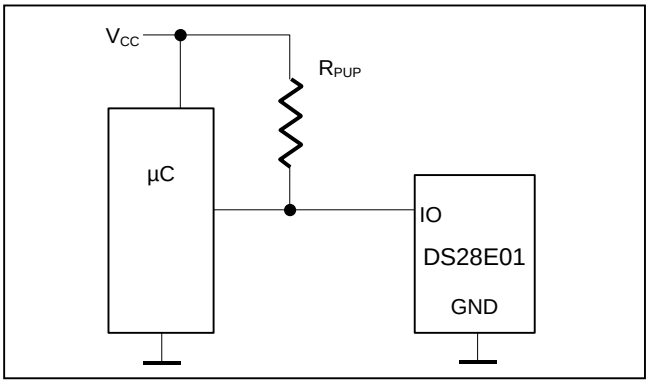
GENERAL DESCRIPTION

The DS28E01-100 combines 1024 bits of EEPROM with challenge-and-response authentication security implemented with the ISO/IEC 10118-3 Secure Hash Algorithm (SHA-1). The 1024-bit EEPROM array is configured as four pages of 256 bits with a 64-bit scratchpad to perform write operations. All memory pages can be write protected, and one page can be put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each DS28E01-100 has its own guaranteed unique 64-bit ROM registration number that is factory lasered into the chip. The DS28E01-100 communicates over the single-contact 1-Wire® bus. The communication follows the standard Dallas Semiconductor 1-Wire protocol with the registration number acting as node address in the case of a multidevice 1-Wire network.

APPLICATIONS

Printer Cartridge Configuration and Monitoring
Medical Sensor Authentication and Calibration
System Intellectual Property Protection

TYPICAL OPERATING CIRCUIT



Commands, Registers, and Modes are capitalized for clarity.

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FEATURES

- **1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits**
- **On-Chip 512-Bit SHA-1 Engine to Compute 160-Bit Message Authentication Codes (MAC) and to Generate Secrets**
- **Write Access Requires Knowledge of the Secret and the Capability of Computing and Transmitting a 160-Bit MAC as Authorization**
- **User-Programmable Page Write Protection for Page 0, Page 3, or All Four Pages Together**
- **User-Programmable OTP EPROM Emulation Mode for Page 1 ("Write to 0")**
- **Communicates to Host with a Single Digital Signal at 15.3kbps or 125kbps Using 1-Wire Protocol**
- **Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise**
- **Reads and Writes Over a Wide Voltage Range of 2.8V to 5.25V from -40°C to +85°C**
- **6-Lead TSOC or 2-Lead SFN Packages**

ORDERING INFORMATION

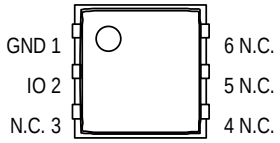
PART	TEMP RANGE	PIN-PACKAGE
DS28E01P-100	-40°C to +85°C	6 TSOC
DS28E01P-100/T&R	-40°C to +85°C	6 TSOC
DS28E01P-100+	-40°C to +85°C	6 TSOC
DS28E01P-100+T&R	-40°C to +85°C	6 TSOC
DS28E01G-100+T&R	-40°C to +85°C	2 SFN

+*Denotes a lead-free package.*
T&R = Tape and reel.

Request full data sheet at:
www.maxim-ic.com/fullds/DS28E01-100

PIN CONFIGURATIONS

TOP VIEW



TSOC (150 mils)

Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

IO Voltage to GND	-0.5V, +6V
IO Sink Current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C; see Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	2.8		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05		6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.46		V_{PUP} - 1.8V	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	1.0		V_{PUP} - 1.1V	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.21		1.70	V
Output Low Voltage	V_{OL}	At 4mA Current Load (Note 11)			0.4	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Time Slot Duration (Note 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
IO PIN, 1-WIRE RESET, PRESENCE DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
IO PIN, 1-Wire WRITE						
Write-0 Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed, V_{PUP} > 4.5V	5		15.5	
		Overdrive speed	6		15.5	
Write-1 Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
IO PIN, 1-Wire READ						
Read Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 19)			0.8	mA
Programming Time	t_{PROG}	(Note 20)			10	ms
Write/Erase Cycles (Endurance) (Notes 21, 22)	N_{CY}	At +25°C	200k			—
		At +85°C (worst case)	50k			
Data Retention (Notes 23, 24, 25)	t_{DR}	At +85°C (worst case)	40			years
SHA-1 ENGINE						
SHA Computation Current (Notes 5, 19)	I_{LCSHA}	Refer to the full version of the data sheet.				mA
SHA Computation Time (Note 5)	t_{CSHA}	Refer to the full version of the data sheet.				ms

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production tested.

Note 2: System requirement.

Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.

Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If R_{PUP} = 2.2kΩ, 2.5µs after V_{PUP} has been applied the parasite capacitance will not affect normal communications.

Note 5: Guaranteed by design, characterization and/or simulation only. Not production tested.

Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is itself a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 7: Voltage below which, during a falling edge on IO, a logic 0 is detected.

Note 8: The voltage on IO needs to be less than or equal to $V_{IL(MAX)}$ at all times the master is driving IO to a logic 0 level.

Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.

Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO has to drop by at least V_{HY} to be detected as logic 0.

Note 11: The I-V characteristic is linear for voltages less than 1V.

Note 12: Applies to a single device attached to a 1-Wire line.

Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.

Note 14: Defines maximum possible bit rate. Equal to $t_{W0L(MIN)} + t_{REC(MIN)}$.

Note 15: Interval after t_{RSTL} during which a bus master is guaranteed to sample a logic 0 on IO if there is a DS28E01-100 present. Minimum limit is $t_{PDH(MAX)}$; maximum limit is $t_{PDH(MIN)} + t_{PDL(MIN)}$.

Note 16: Highlighted numbers are NOT in compliance with legacy 1-Wire product standards. See comparison table below.

Note 17: ε in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1L(MAX)} + t_F - \varepsilon$ and $t_{W0L(MAX)} + t_F - \varepsilon$, respectively.

Note 18: δ in Figure 12 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RL(MAX)} + t_F$.

Note 19: Current drawn from IO during EEPROM programming or SHA-1 computation interval.

Note 20: Refer to the full version of the data sheet.

Note 21: Write-cycle endurance is degraded as T_A increases.

Note 22: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 23: Data retention is degraded as T_A increases.

Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.

Note 25: EEPROM writes may become nonfunctional after the data-retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device may lose its write capability after 10 years at +125°C or 40 years at +85°C.

PARAMETER	LEGACY VALUES				DS28E01-100 VALUES			
	STANDARD SPEED		OVERDRIVE SPEED		STANDARD SPEED		OVERDRIVE SPEED	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undef.)	7µs	(undef.)	65µs[1)]	(undef.)	8µs[1)]	(undef.)
t_{RSTL}	480µs	(undef.)	48µs	80µs	480µs	640µs	48µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	60µs	2µs	6µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	240µs	8µs	24µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	6µs	15.5µs

[1)] Intentional change, longer recovery time requirement due to modified 1-Wire front-end.

PIN DESCRIPTION

PIN (TSOC)	NAME	FUNCTION
1	GND	Ground Reference
2	IO	1-Wire Bus Interface. Open drain, requires external pullup resistor.
3–6	N.C.	Not Connected

DESCRIPTION

The DS28E01-100 combines 1024 bits of EEPROM organized as four 256-bit pages, a 64-bit secret, a register page, a 512-bit SHA-1 engine, a 64-bit ROM registration number in a single chip. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return. The DS28E01-100 has an additional memory area called the scratchpad that acts as a buffer when writing to the memory, the register page, or when installing a new secret. Data is first written to the scratchpad from where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to its final memory location, provided that the DS28E01-100 receives a matching 160-bit MAC. The computation of the MAC involves the secret and additional data stored in the DS28E01-100 including the device's registration number. Only a new secret can be loaded without providing a MAC. The SHA-1 engine is also activated to compute 160-bit MACs when performing an authenticated read of a memory page and when computing a new secret, instead of loading it.

The DS28E01-100 understands a unique command "Refresh Scratchpad." Proper use of a refresh sequence after a copy scratchpad operation reduces the number of weak bit failures if the device is used in a touch environment (see the *Writing with Verification* section). The refresh sequence also provides a means to restore functionality in a device with bits in a weak state.

The device's 64-bit ROM registration number guarantees unique identification and is used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. Applications of the DS28E01-100 include printer cartridge configuration and monitoring, medical sensor authentication and calibration, and system intellectual property protection.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E01-100. The DS28E01-100 has six main data components: 1) 64-bit lasered ROM, 2) 64-bit scratchpad, 3) four 256-bit pages of EEPROM, 4) register page, 5) 64-bit secrets memory, and 6) a 512-bit SHA-1 (Secure Hash Algorithm) engine. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Resume Communication, 6) Overdrive-Skip ROM, or 7) Overdrive-Match ROM. Upon completion of an overdrive ROM command byte executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 10. After a ROM function command is successfully executed, the memory and SHA-1 functions become accessible and the master can provide any one of the 9 available function commands. The function protocols are described in Figure 8*. **All data is read and written least significant bit first.**

*For Figure 8, refer to the full version of the data sheet.

Figure 1. Block Diagram

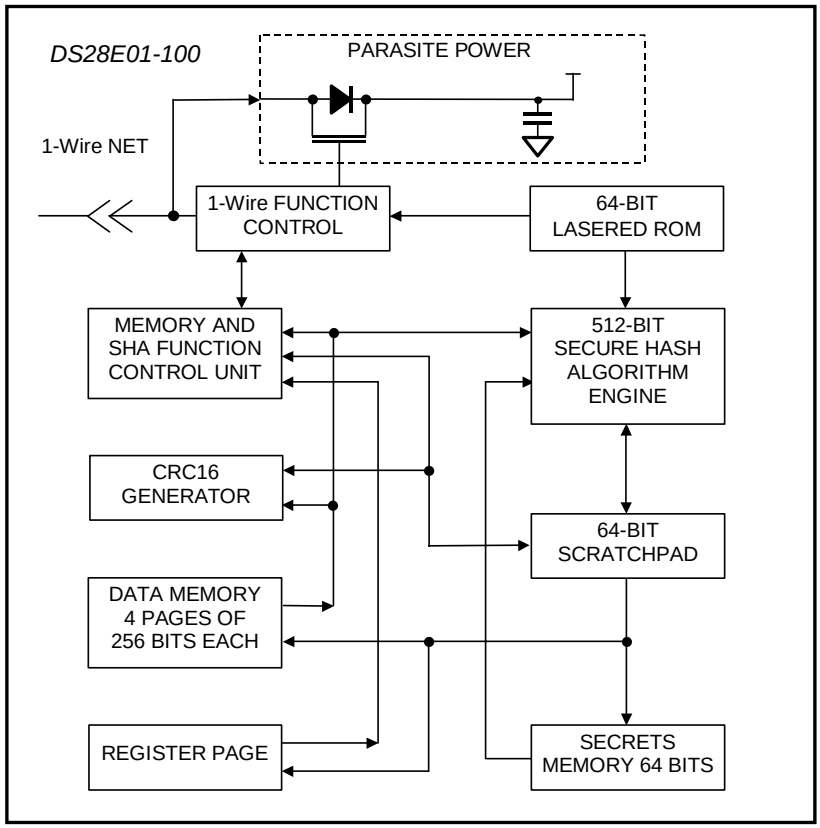
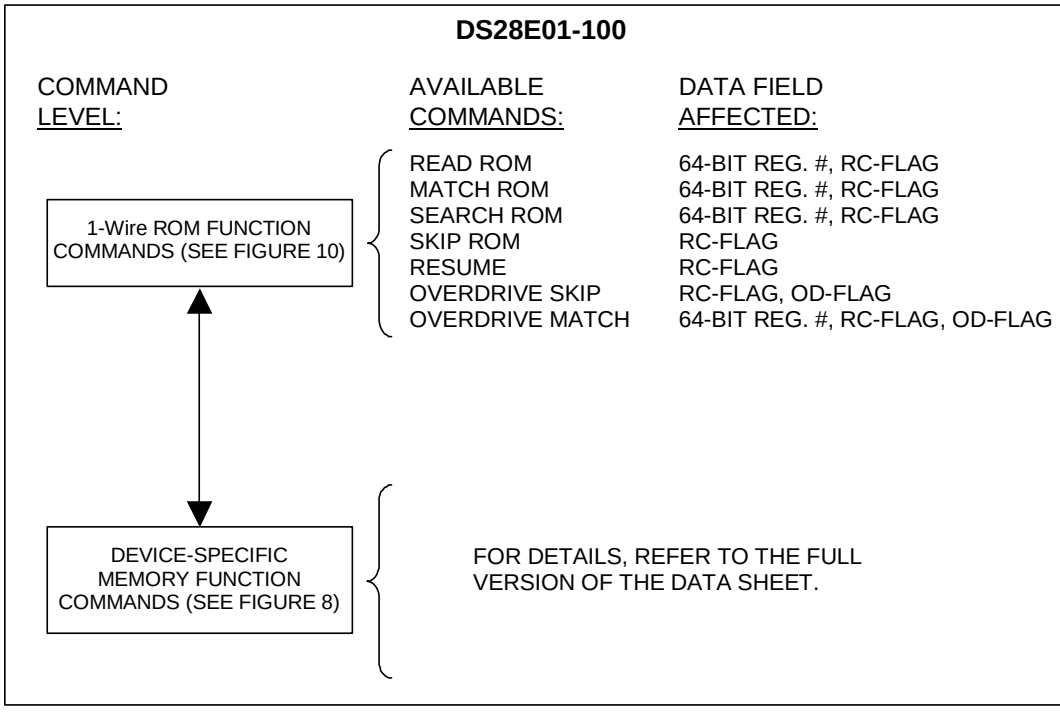


Figure 2. Hierarchical Structure for 1-Wire Protocol



64-BIT LASERED ROM

Each DS28E01-100 has a unique ROM Registration Number that is 64 bits long, as shown in Figure 3. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC (Cyclic Redundancy Check) of the first 56 bits. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire CRC is available in *Application Note 27*. The shift register bits are initialized to zero. Then starting with the LSB of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

Figure 3. 64-Bit Lasered ROM

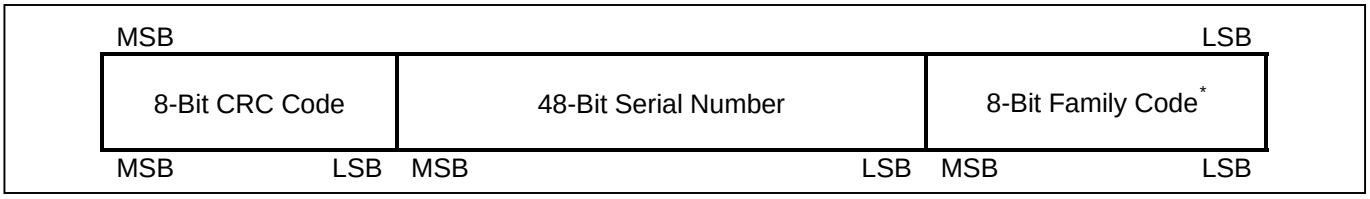
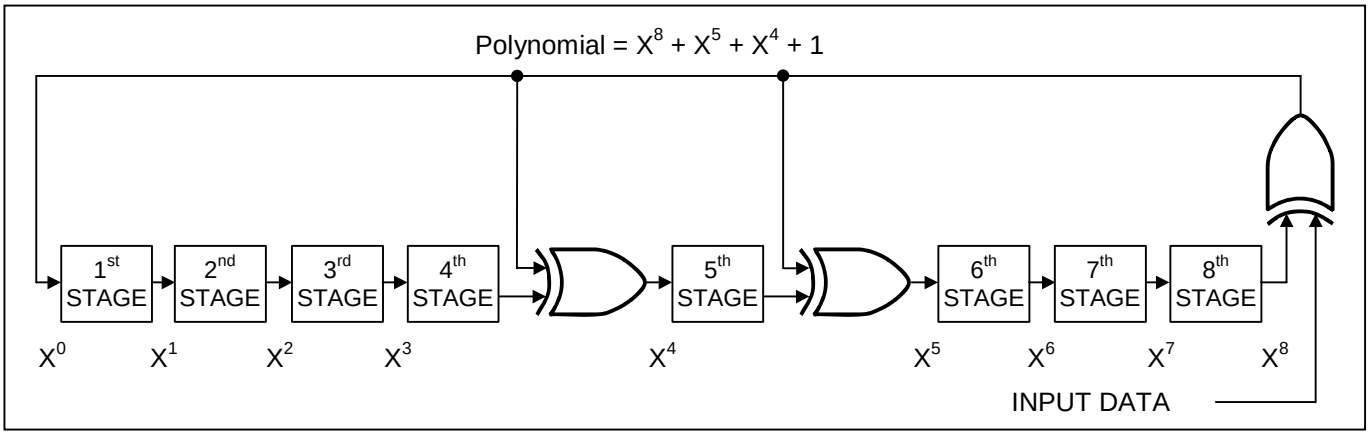


Figure 4. 1-Wire CRC Generator



MEMORY

The DS28E01-100 has four memory areas: data memory, secrets memory, register page with special function registers and user bytes, and a volatile scratchpad. The data memory is organized as four pages of 32 bytes. Secret and scratchpad are 8 bytes each. The scratchpad acts as a buffer when writing to the data memory, loading the initial secret or when writing to the register page. For further details (including Figures 5 and 6) refer to the full version of the data sheet.

* For the actual Family Code refer to the full version of the data sheet.

ADDRESS REGISTERS AND TRANSFER STATUS

The DS28E01-100 employs three address registers: TA1, TA2, and E/S (Figure 7). These registers are common to many other 1-Wire devices but operate slightly differently with the DS28E01-100. Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read-only transfer-status register, used to verify data integrity with write commands. Since the scratchpad of the DS28E01-100 is designed to accept data in blocks of eight bytes only, the lower three bits of TA1 are forced to 0 and the lower three bits of the E/S register (ending offset) always read 1. This indicates that all the data in the scratchpad is used for a subsequent copying into main memory or secret. Bit 5 of the E/S register, called PF or partial byte flag, is a logic 1 if the number of data bits sent by the master is not an integer multiple of eight or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad clears the PF bit. Bits 3, 4, and 6 have no function; they always read 1. The partial flag supports the master checking the data integrity after a write command. The highest valued bit of the E/S register is called the AA or authorization accepted flag, which indicates that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

Figure 7. Address Registers

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2 (0)	T1 (0)	T0 (0)
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	1	PF	1	1	E2 (1)	E1 (1)	E0 (1)

WRITING WITH VERIFICATION

To write data to the DS28E01-100, the scratchpad has to be used as intermediate storage. First the master issues the write scratchpad command, which specifies the desired target address and the data to be written to the scratchpad. Note that writes to data memory must be performed on 8-byte boundaries with the three LSBs of the target address T2–T0 equal to 000b. Therefore, if T2–T0 are sent with nonzero values, the device sets these bits to zero and uses the modified address as the target address. The master should always send eight complete data bytes. After the eight bytes of data have been transmitted, the master can elect to receive an inverted CRC16 of the write scratchpad command, the address as sent by the master, and the data as sent by the master. The master can compare the CRC to the value it has calculated itself in order to determine if the communication was successful. After the scratchpad has been written, the master should always perform a read scratchpad to verify that the intended data was in fact written. During a read scratchpad, the DS28E01-100 repeats the target address TA1 and TA2 and sends the contents of the E/S register. The partial flag (bit 5 of the E/S register) is set to 1 if the last data byte the DS28E01-100 received during a write scratchpad or refresh scratchpad command was incomplete, or if there was a loss of power since data was last written to the scratchpad. The authorization-accepted (AA) flag (bit 7 of the E/S register) is normally cleared by a write scratchpad or refresh scratchpad; therefore, if it is set to 1, it indicates that the DS28E01-100 did not understand the proceeding write (or refresh) scratchpad command. In either of these cases, the master should rewrite the scratchpad. After the master receives the E/S register, the scratchpad data is received. The descriptions of write scratchpad and refresh scratchpad provide clarification of what changes can occur to the scratchpad data under certain conditions. An inverted CRC of the read scratchpad command, target address, E/S register, and scratchpad data follows the scratchpad data. As with the write scratchpad command, this CRC can be compared to the value the master has calculated itself in order to determine if the communication was successful. After the master has verified the data, it can send the copy scratchpad to copy the scratchpad to memory. Alternatively, the load first secret or compute next secret command can be issued to change the secret. See the descriptions of these commands for more information.

MEMORY AND SHA FUNCTION COMMANDS

This section describes the commands and flowcharts to use the memory and SHA-1 engine of the device. It includes Tables 1 to 4 and Figure 8. Refer to the full version of the data sheet.

SHA-1 COMPUTATION ALGORITHM

This description of the SHA computation is adapted from the Secure Hash Standard SHA-1 document that can be downloaded from the NIST website (www.itl.nist.gov/fipspubs/fip180-1.htm). Further details are found in the full version of the data sheet.

1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28E01-100 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

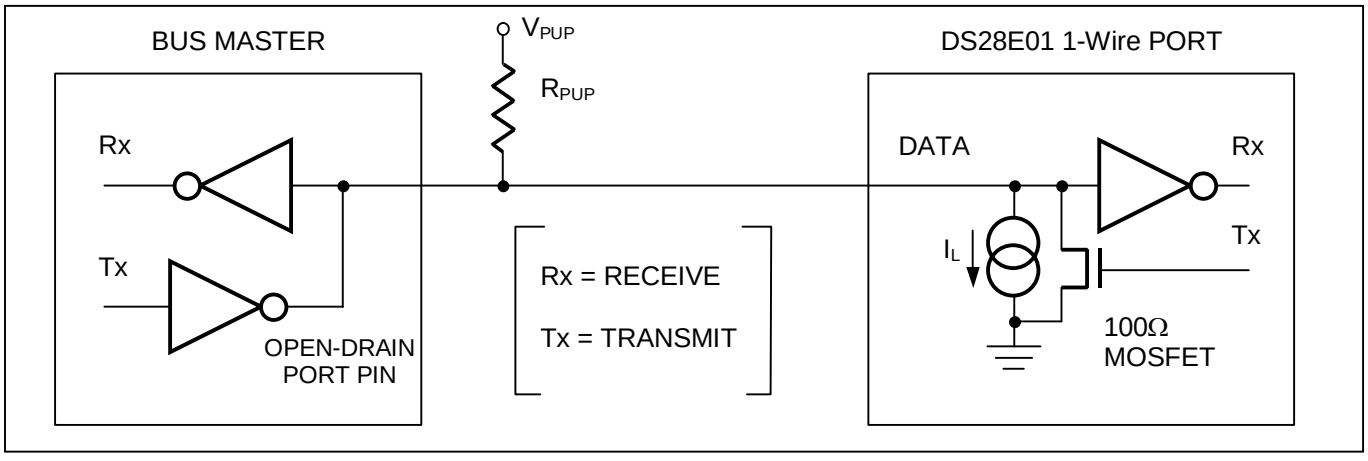
HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E01-100 is open drain with an internal circuit equivalent to that shown in Figure 9.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E01-100 supports both a Standard and Overdrive communication speed of 15.3kbps (max) and 125kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and Overdrive of 142kbps. The slightly reduced rates for the DS28E01-100 are a result of additional recovery times, which in turn were driven by a 1-Wire physical interface enhancement to improve noise immunity. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E01-100 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (Overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset.

Figure 9. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS28E01-100 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/SHA Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E01-100 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E01-100 supports. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 10).

READ ROM [33h]

This command allows the bus master to read the DS28E01-100's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

MATCH ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E01-100 on a multidrop bus. Only the DS28E01-100 that exactly matches the 64-bit ROM sequence, including the external address, responds to the following Memory/Control Function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their device ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the device ID numbers of all slave devices. For each bit of the device ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its device ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its device ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the device ID number of a single device. Additional passes identify the device ID numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

SKIP ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Figure 10A. ROM Functions Flowchart

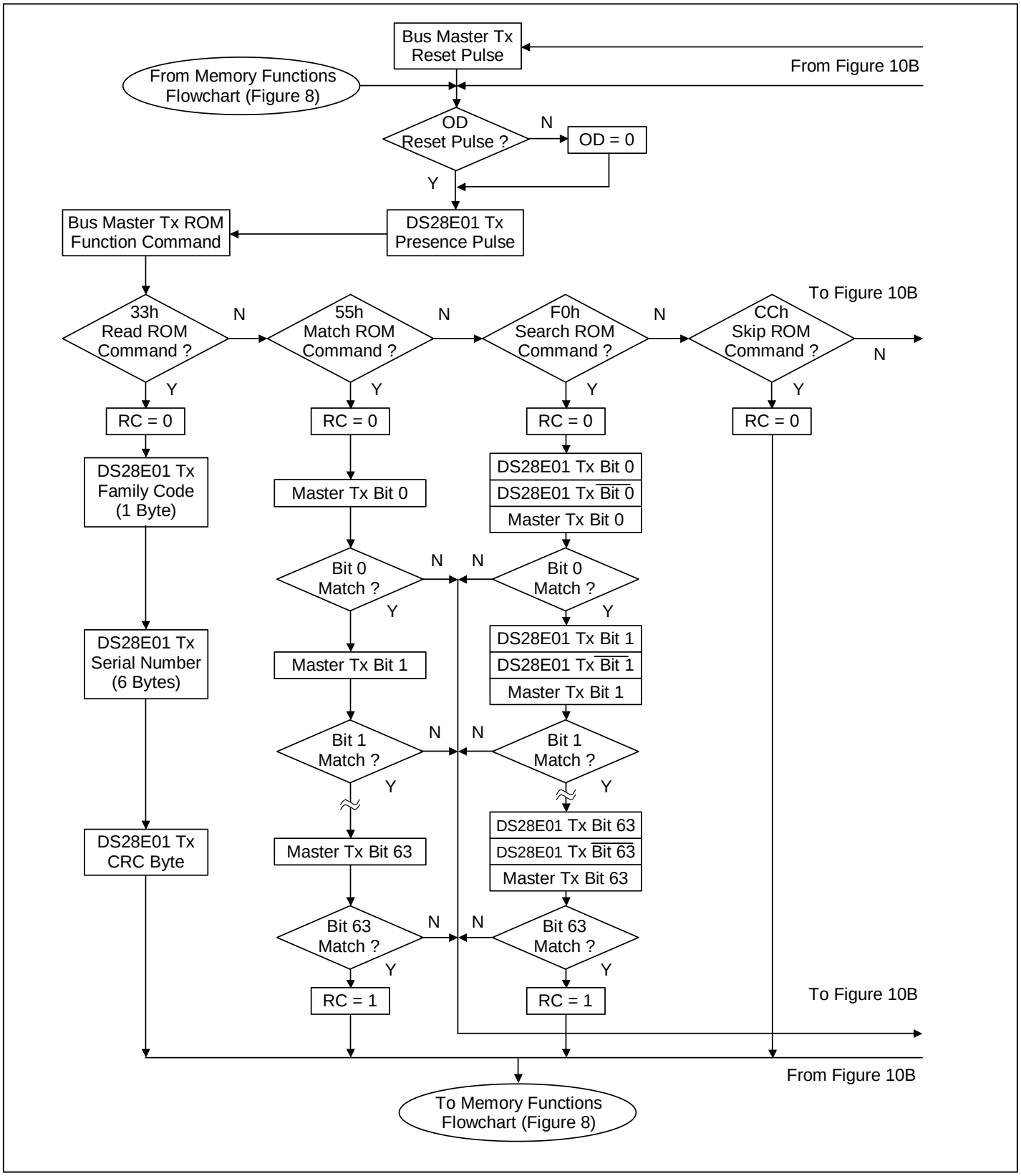
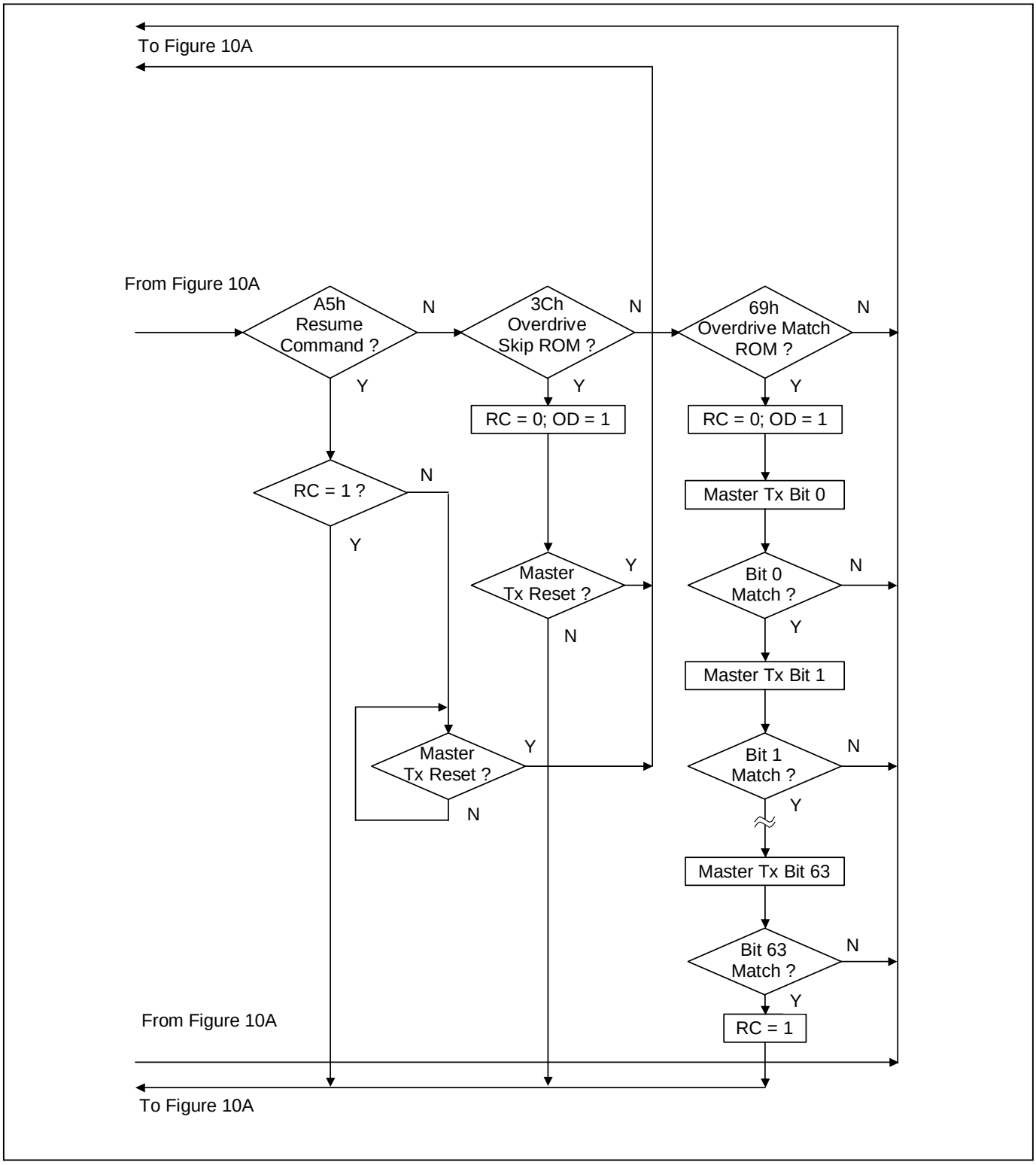


Figure 10B. ROM Functions Flowchart (continued)



RESUME [A5h]

To maximize the data throughput in a multidrop environment, the Resume function is available. This function checks the status of the RC bit and, if it is set, directly transfers control to the Memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume Command function.

OVERDRIVE SKIP ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS28E01-100 in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at Overdrive Speed allows the bus master to address a specific DS28E01-100 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS28E01-100 that exactly matches the 64-bit ROM sequence responds to the subsequent Memory or SHA Function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

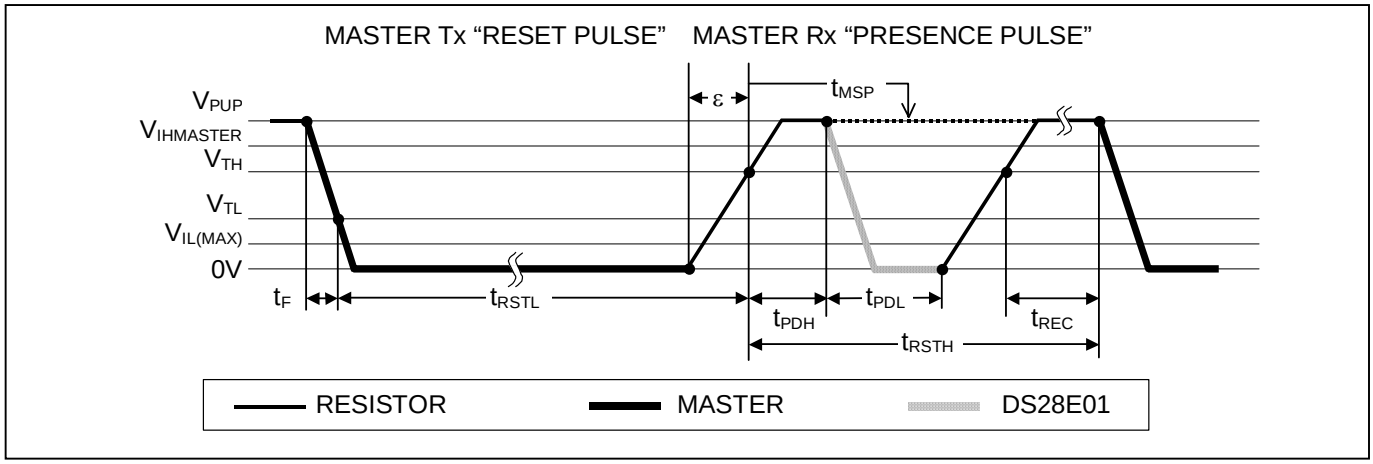
1-Wire SIGNALING

The DS28E01-100 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the Presence pulse, the bus master initiates all falling edges. The DS28E01-100 can communicate at two different speeds, standard speed, and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS28E01-100 communicates at standard speed. While in Overdrive Mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from $V_{IL(MAX)}$ past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 11 as "ε" and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage $V_{IL(MAX)}$ is relevant for the DS28E01-100 when determining a logical level, not triggering any events.

Figure 11 shows the initialization sequence required to begin any communication with the DS28E01-100. A Reset Pulse followed by a Presence Pulse indicates the DS28E01-100 is ready to receive data, given the correct ROM and Memory/Control Function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive Mode, returning the device to standard speed. If the DS28E01-100 is in Overdrive Mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive Mode. If the device is in Overdrive Mode and t_{RSTL} is *between* 80µs and 480µs, the device will reset, but the communication speed is undetermined.

Figure 11. Initialization Procedure: Reset and Presence Pulse



After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in case of a DS2482-x00 or DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS28E01-100 waits for t_{PDH} and then transmits a Presence Pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of $t_{PDH(MAX)}$, $t_{PDL(MAX)}$, and $t_{REC(MIN)}$. Immediately after t_{RSTH} is expired, the DS28E01-100 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at Overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS28E01-100 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 12 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E01-100 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Figure 12. Read/Write Timing Diagram

Write-One Time Slot

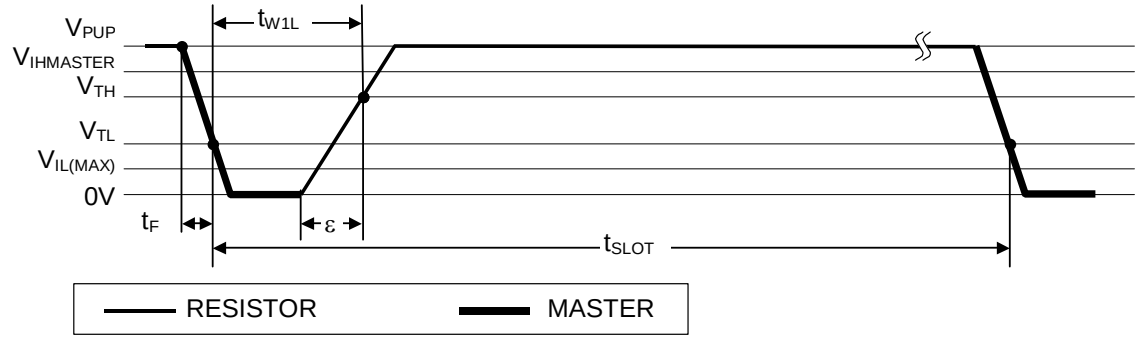
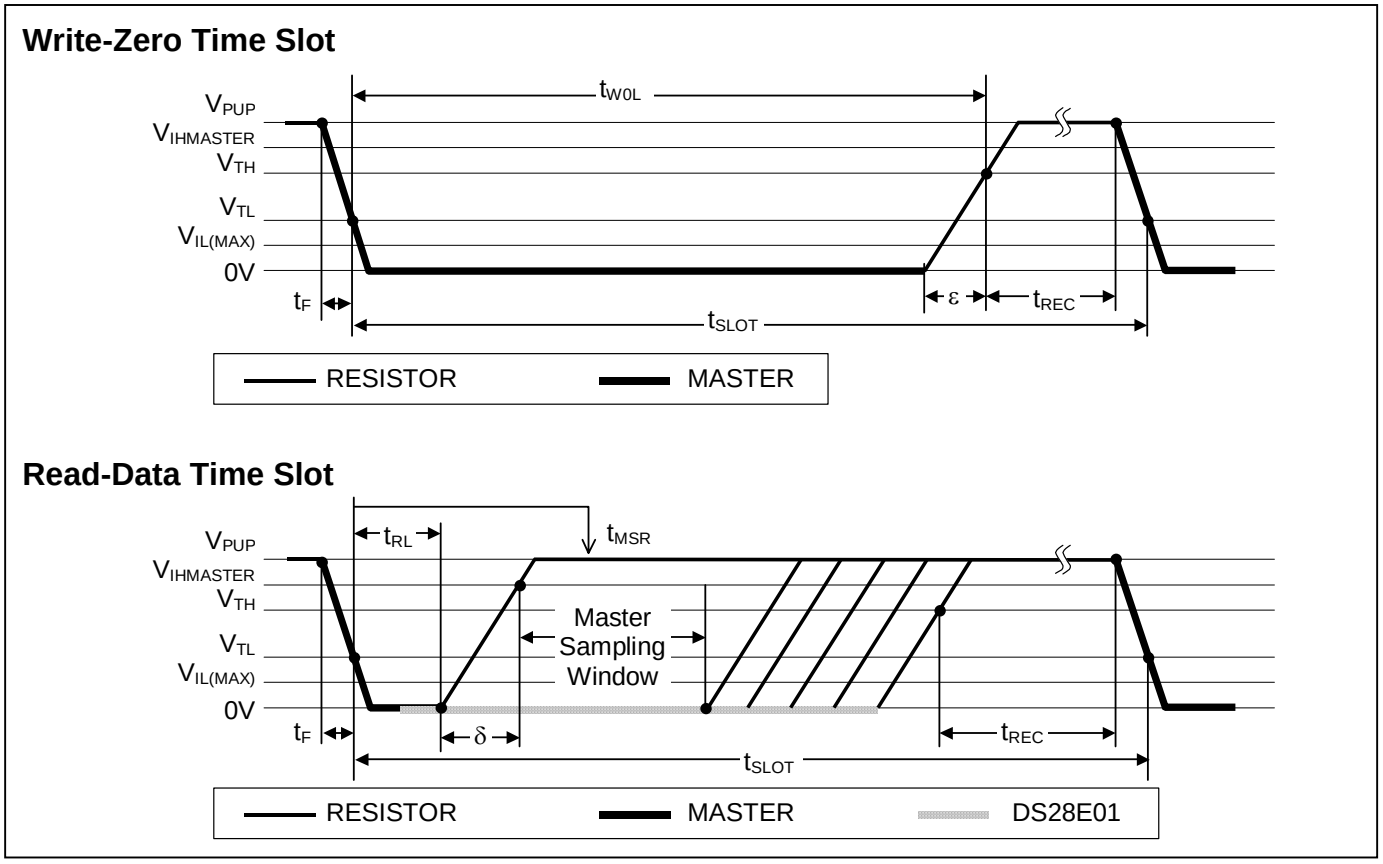


Figure 12. Read/Write Timing Diagram (continued)



Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time $t_{W1L(MAX)}$ is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed $V_{IL(MAX)}$ during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E01-100 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E01-100 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E01-100 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E01-100 on the other side define the master sampling window ($t_{MSR(MIN)}$ to $t_{MSR(MAX)}$) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than $t_{MSR(MAX)}$. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E01-100 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E01-100 attached to a 1-Wire line. For multidevice configurations, t_{REC} needs to be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

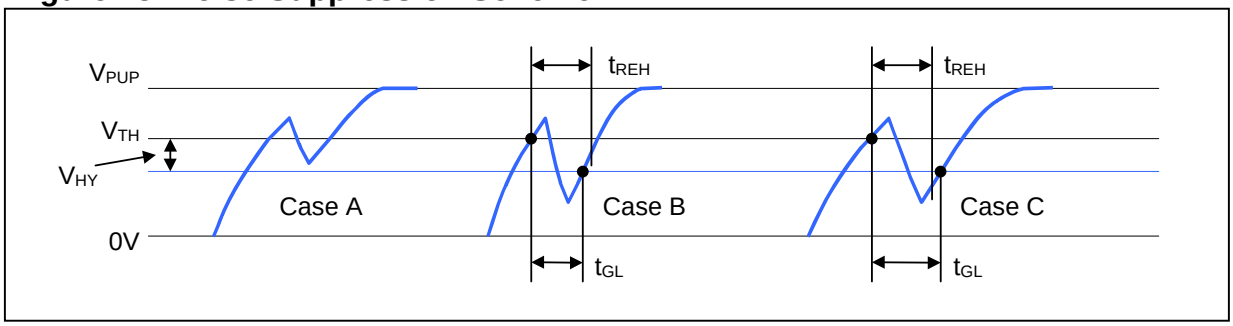
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up, or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E01-100 uses a new 1-Wire front-end, which makes it less sensitive to noise.

The 1-Wire front-end of the DS28E01-100 differs from traditional slave devices in three characteristics.

1) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at Overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it will not be recognized (Figure 13, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below V_{TH} - V_{HY} threshold (Figure 13, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 13, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters V_{HY}, and t_{REH} specified in their electrical characteristics use the improved 1-Wire front-end.

Figure 13. Noise Suppression Scheme

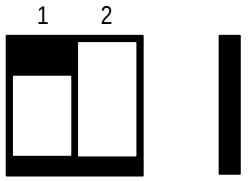


CRC GENERATION

With the DS28E01-100 there are two different types of CRCs. One CRC is an 8-bit type. It is computed at the factory and is stored in the most significant byte of the 64-bit ROM. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. To determine whether the ROM data has been read without error the bus master can compute the CRC value from the first 56 bits of the 64-bit ROM and compare it to the value read from the DS28E01-100. This 8-bit CRC is received in the true form (noninverted) when reading the ROM.

The other CRC is a 16-bit type, which is used for error detection with Memory and SHA-1 function commands. For details (including Figure 14) refer to the full version of the data sheet.

PIN CONFIGURATIONS (continued)

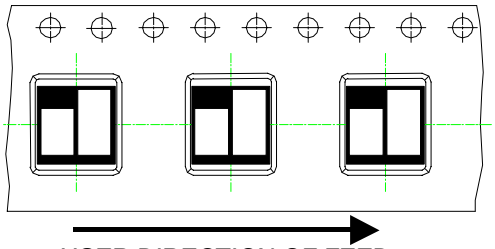


SFN PINOUT:
PIN 1: IO
PIN 2: GND

SFN (APPROX. 6.0mm x 6.0mm x 0.9mm)

NOTE: THE SFN PACKAGE IS QUALIFIED FOR ELECTRO-MECHANICAL CONTACT APPLICATIONS ONLY, NOT FOR SOLDERING. FOR MORE INFORMATION, REFER TO *APPLICATION NOTE 4132: ATTACHMENT METHODS FOR THE ELECTRO-MECHANICAL SFN PACKAGE*.

SFN PACKAGE ORIENTATION ON TAPE AND REEL



USER DIRECTION OF FEED

LEADS FACE UP IN ORIENTATION SHOWN ABOVE.

PACKAGE INFORMATION

(For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 TSOC	—	**56-G2016-001**
2 SFN	—	**56-00SFN-000**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
040907	Initial release.	—
071207	In the SFN Pin Configuration, added the package drawing information/weblink and a note that the SFN package is qualified for electro-mechanical contact applications only, not for soldering. Added the SFN Package Orientation on Tape-and-Reel section. In the Ordering Information, added note to contact factory for availability of the UCSP package.	16
032008	Removed references to the UCSP package.	1, 16
	In the SFN Pin Configuration, added reference to Application Note 4132.	16

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